Anomalous Phenomena on Subthreshold Characteristics of SOI MOSFET Back Gate Voltage

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SOI MOSFET Back게이트 전압에 따른 Subthreshold 특성의 특수현상
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Abstract
The 1-D numerical model and its extraction methodology are suggested and these simulation results for the S-swing as a function of back-gate voltage are well matched with the measured. S-swing characteristics are analyzed using PD-SOI devices with enough deeper regions up to substrates. The PD-SOI device doesn’t have to be short channel to see the anomalous subthreshold phenomena based on the back gate bias. This results recommend to operate better SOI device performances by controlling the back gate voltages. So SOI performances will be much optimistic with proper control of the back-gate voltage for the already-proven-high-performance(APHP) SOI VLSIs.

2. Model Development of SOI MOSFET

1) Necessity of the numerical model
SOI process technology has recently matured to improve the performances. However there are some unsolved problems for variations of SOI silicon thickness, gate oxide uniformity high substrate costs and floating body mechanisms. Commercial products using SOI VLSIs to those problems against conventional bulk-Si SOI VLSIs. There are two types of SOI CMOS: one is Partially Depleted(PD); the other Fully-Depleted (FD)[1]. These SOI types are classified by processing technology, varying a formentioned SOI parameters. Currently possible commercial products are mainly made out of the PD-SOI CMOS[2]. Another thrust for SOI researches so far is focused on deep submicron high performance FD-SOI design, varying thin gate oxide and thin SOI silicon thickness, but leakage currents and reliability issues by FD-SOI design causes the gate oxide uniformity and bleeding power at low voltage operation. It is so important that S-swing characteristic must be analyzed using PD-SOI devices with enough deeper regions up to substrates. The PD-SOI device doesn’t have to be short channel to see the anomalous subthreshold phenomena based on the back gate bias. First, there are many analytical and numerical models to evaluate device characteristics and verifications of valid parameter fittings, but those analytical & numerical models can not include the effect of bulk substrate, and just approximates the potential distribution within the substrate. Therefore, accurate 1-D numerical model is constructed to see the effect of SOI’s backgate voltage for S-swing. The model
converges fast and simulation time is short. Based on the result of the simulation model, structural parameter extraction of the SOI MOSFET shows the fundamental extraction methodology using 1-D numerical model with various physical characteristics.

2) Basic Mathematical Formulations
The 1-D numerical equations of the SOI MOSFET are eq. (1), (2), (3) and (4). These poisson’s and related continuity equations calculate the region of subthreshold and then election concentrations, and hole concentrations will be evaluated using the thermal equilibrium states.

\[
\frac{d}{dx} \left( e \frac{dn}{dx} \right) = -q(N_N - n(x) + p(x)) \tag{1}
\]

\[
n(x) = \frac{m_i}{e} \frac{1}{\sqrt{4\pi k_B T_0}} e^{\left(\frac{qV(x)}{k_B T_0}\right)} \tag{2}
\]

\[
p(x) = \frac{m_i}{e} \frac{1}{\sqrt{4\pi k_B T_0}} e^{\left(\frac{qV(x) + V_{th}}{k_B T_0}\right)} \tag{3}
\]

\[
p(x) = \frac{m_i}{n(x)} \tag{4}
\]

Where \( N_N \) is impurity concentration of SOI layer, is a thermal voltage as 25.9mV. Fig.1 shows the cross-sectional of SOI MOSFET for the simulations. As shown in Fig.1, considered PD-SOI parameters including the substrate are gate oxide thickness, SOI layer thickness, buried-oxide thickness, bulk substrate thickness, SOI layer's doping concentrations, bulk substrate impurity concentration. Based on the model with various SOI parameters, surface potentials, surface trapped states, gate voltage and bulk substrate voltages are calculated with proper boundary conditions as:

\[
V_{g} = V_{gf} - \Phi_{gate} \tag{5}
\]

\[
V_{b} = V_{gb} - \Phi_{sub} \tag{6}
\]

Where \( \Phi_{gate} \) is potential difference between SOI layer and n-type poly silicon and is about -0.8V, \( \Phi_{sub} \) is Fermi voltage difference between SOI layer and bulk substrate, \( \Phi_{sub} = \frac{kT_0}{q} \log \left( \frac{N_{sub}}{N_i} \right) \) and \( N_{sub} \) is bulk substrate density.

3) Surface Trapped States Model
Interface trapped states are analyzed from the interface trap distribution along with Fermi-dirac distribution formula as the below Eqs[1-3]:

\[
F_{SA} (E_i) = \frac{1}{1 + g e^{\left( \frac{E_i - E_{tr}}{kT} \right)}} \tag{7}
\]

\[
F_{SB} (E_i) = \frac{1}{1 + e^{\left( \frac{E_i - E_{tr}}{kT} \right)}} \tag{8}
\]

\[
Q_{n,0,2,3} = \int_{0}^{1} (D_{n,0,2,3} F_{SB} - D_{n,0,2,3} F_{SA} + D_{n,0,2,3} D_{n,0,2,3}) dE_i + Q_{n,0,2,3} \tag{9}
\]

4. Results, Discussions and Summary
Performances and characteristics of SOI MOSFET generally depend on various parameters such as SOI thickness(t_{SOI}), front gate oxide(t_{ox}), buried oxide thickness(t_{iox}), impurity concentration(N_A or N_{sub}), and surface interface states(D_{s1},D_{s2},D_{s3}). It is well-known that SOI has excellent advantages over Bulk-Si MOS for future low power and high speed ULSIS[2]. Analysis and optimization of the electrical properties of SOI, however, need some actual parameter for development of the fundamental device performance. Plane numerical model and model parameters with device capacitances of partially depleted(PD)-SOI MOSFET are shown in Fig. 1(a),(b) where the oxide of (100) p-type substrate is 4X10^6/4m, expected fabricated values of t_{ox} t_{sox} t_{iox} are 7, 50, and 80nm, respectively. The sampled gate length and width of the PD SOI are 1 and 20um[3] to understand the subthreshold slope factor(S-swing) characteristics by varying back gate voltages[4]-[6]. This research presents thorough S-swing phenomena by the gate bias voltages for better performance of better S-swing region. Fig. 2(a),(b) show measured and simulated drain-gate characteristics as a function of backgate voltage in the region of subthreshold. Fig. 2 looks a normal subthreshold characteristics [7][8] without indicating parasitic MOS effect of edge area of SOI silicon layer, i.e., drain currents above the back gate voltages of 2V is not decreasing up to measured critical limit and indicate a constant value of the drain currents because the back channel is generated due to inversion at the boundary of SOI silicon layer[9]. Fig. 3(a),(b) show the numerical and measured results for the S-swing as a function of back gate voltages where the region I is acc. of SOI layer, II is complete dep. toward SOI layer, III weak inv. of the SOI layer, IV weak inv. of the SOI layer with acc. from dep. at the bulk substrate, and V sharp increase of S-swing since there is no way to control the front gate when the back channel is generated. From the Fig. 3, unlike normal MOS, the S-swing shows anomalous phenomenon of boundaries at each layer. Further electron and hole density explain these regions as shown in Fig. 4(a),(b). D_{s1}- and D_{s2}-dependence by the back gate voltage clearly, for the first time to date, reveal local minima of the S-swing whose values largely varies, depending on the D_{s1}- and D_{s2}-variation. As shown in Fig. 5(a), (b), the numerical calculations match with the measured results from various samples where extracted parameter sets are listed as Table 1. This results recommend to operate better SOI device performances by controlling the back gate voltages. Further, validity of characteristics from various fitting parameters is analyzed by least square error method based on the following eq:n

\[
\Delta = \sum \left( S_m \left( V_{BS} \right) - S_t \left( V_{BS} \right) \right) \times a(S) \right)^2.
\]

where w(S) is weighted factor, Sm and St are
S-swing of measured and simulation. Fig. 6 show the valid contour plot for local minimum for each parameters.

References


Table 1. Extracted parameter sets for S-swing

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sample 1</th>
<th>Sample 2</th>
<th>Sample 3</th>
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<tr>
<td>$g_{xx}$ (nA)</td>
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<td>6.0</td>
<td>7.3</td>
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<td>$t_{soi}$ (nm)</td>
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<td>$t_{ox}$ (nm)</td>
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<td>$N_{d}$ (cm$^{-3}$)</td>
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<td>$1 \times 10^{15}$</td>
<td>$1 \times 10^{14}$</td>
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<tr>
<td>$N_{a}$ (cm$^{-3}$)</td>
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<td>$8 \times 10^{15}$</td>
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<tr>
<td>$D_{d}$ (cm$^{-2}$ eV$^{-1}$)</td>
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<td>$5 \times 10^{10}$</td>
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<td>$Q_{d}$ (cm$^{-2}$)</td>
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<td>$Q_{a}$ (cm$^{-2}$)</td>
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<td>$8 \times 10^{11}$</td>
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Fig.1(a) SOI device view. (b) PD SOI device capacitances

Fig.2(a) Measured I-V as a function of front gate voltage.

Fig.3(a) S-swing characteristics as a function of back gate voltage. (b) Magnified portion of (a).
Fig. 4. Electron density for S-swing characteristics of (a) SOI thickness depth, (b) substrate depth, (c) Hole density for S-swing characteristics of thickness depth, (d) of substrate depth.

Fig. 5(a) Di2-dependence of S-swing characteristics, (b) Di3-dependence of S-swing characteristics, (c) A typical Di3-dependence of S-swing characteristics with measured ones, (d) A typical Di3-dependence of S-swing characteristics with measured ones.

Fig. 6(a) The valid contour plots for local minimum for each parameters as a error analyses in (a) (Di2, Nsub)-space, (b) (Di3, Nsub)-space, (c) (Q12, Q13)-space, and (d) (T_{SOI}, T_{box})-space.