Implementation of IIR Notch Filter on FPGA


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Abstract: This paper proposes the implementation of IIR notch filter onto FPGA (Field Programmable Gate Array), which is an integrated circuit that allows user to reprogram it after manufacturing. The advantages of FPGA notch filter, compared to software filter, are stability, speed, precision and ability of narrowed bandwidth filter implementation. The IIR notch filter algorithm using in this research is the modified least square estimation that places Pole-zero on z-plane and assigns the amplification level of pass-band gain. The 32-bit floating point is also used in this implementation to maximize the precision of FPGA calculation. By experiments, this FPGA notch filter is able to produce very high precision frequency response between 1 Hz - 5 MHz and is able to function in very narrowed bandwidth (≥ 1 Hz).

Keywords: FPGA, Field Programmable Gate Array, DSP, IIR notch filter, least square estimation

1. INTRODUCTION

Digital Signal Processing, especially in the field of FPGA (Field Programmable Gate Array), is one of the fastest developed areas in today’s technology Electronics. Rather than fitting the algorithm to the architecture as general-purpose DSP, FPGA fits the architecture to the algorithm that makes it the ideal platform for DSP implementation. It combines the reprogrammability, architectural flexibility and customizability that allow the system designers to suite any processing purposes. Recently, hundreds of FPGA applications have been introduced in many engineering fields such as Digital Control, Data compression, Image Processing, Signal processing, and biomedical signal processing and etc.

For signal processing, IIR filter is the recursive filter, which has poles on unit circle instead on the origin as non-recursive filter [2]. The unit circle position of IIR filter’s pole enables it to be constructed as a narrow bandwidth band-pass filter (or notch filter). Placing pole-zero on z-plane is the easiest way to implement IIR notch filter but it will be limited by uncontrollable size and asymmetrical pattern of pass-band gain [1, 3].

This paper applies the least square approximation technique to overcome the limitation in pass-band gain of pole-zero placements on z-plane. This improved algorithm uses floating point calculation to enhance the precision and accuracy of band-pass narrowing and enable the designed IIR notch filter to remove noises at any specified frequencies. The elimination of very narrow bandwidths is really required in high precision equipment such as measuring instruments and medical instruments.

2. IIR NOTCH FILTER

The frequency response specification of ideal single notch filter is given by

\[ H(e^{j\omega}) = \begin{cases} 0 & \omega = \omega_n \\ 1 & \text{otherwise} \end{cases} \]  \hspace{1cm} (1)

\( \omega_n \) is the cut-off frequency of notch filter.

And the transfer function of this ideal single notch filter is shown as follows:

\[ H(z) = b_0 \frac{1 - 2\cos(\omega_n z^{-1}) + z^{-2}}{1 - 2r \cos(\omega_n z^{-1}) + r^2 z^{-2}} \]  \hspace{1cm} (2)

\( b_0 \) is filter gain.

\( \omega_n \) is pole-zero angle on z plane

or cut-off frequency

or notch frequency.

\( r \) is distance between pole and the origin.

From the magnitude Response of the IIR Notch Filter of Eq. (2) shown in Fig. 1, the pass-band is not only asymmetric but also unable to be adjusted to the designed range.

![Fig. 1 The magnitude response of the ideal single notch filter](image)

The asymmetrical pattern of the pass-band frequencies comes from the inappropriate values of \( \omega_n \) and the inappropriate positions of the pole. Therefore, it is necessary to adjust the values of \( \omega_n \) and the poles’ positions to make the pass-band symmetry. The changing of \( b_0 \) is also required to improve the gain of pass-band frequencies [4].

\( \omega_n \) is assigned as the changing cut-off frequency \( \omega_n + \phi \) as shown in Eq. (3).

\[ \hat{\omega}_n = \omega_n + \phi \]  \hspace{1cm} (3)

The value of \( \phi \) is calculated from Eq. (4)
While the value of $b_0$ can be estimated by the Least Square Estimation technique [5] as shown in Eq. (5).

$$b_0 = -\frac{k(a_1 + a_2)}{a_1^2 + a_2^2}$$

$$a_1 = \frac{1 - 2\cos\omega_n e^{-i\theta} + e^{-2i\theta}}{1 - 2r\cos\omega_n e^{-i\theta} + r^2 e^{-2i\theta}}$$

$$a_2 = \frac{1 - 2\cos\omega_n e^{-i\phi} + e^{-2i\phi}}{1 - 2r\cos\omega_n e^{-i\phi} + r^2 e^{-2i\phi}}$$

$k$ is the Gain at pass-band

From Eqs. (3) ~ (6), the transfer function of IIR Notch Filter can be rewritten as improved transfer function, $\hat{H}(z)$ as shown in Eq. (7) which has the magnitude response presented in Fig. 2.

$$\hat{H}(z) = b_0 \left[ \frac{1 - 2\cos\omega_n z^{-1} + z^{-2}}{1 - 2r\cos\omega_n z^{-1} + r^2 z^{-2}} \right]$$

The bandwidth of IIR Notch filter can be calculated by using geometrical properties as shown in Eq. (8).

$$\Delta\omega = 2(1 - r)$$

### 3. IMPLEMENTATION

We start from the improved transfer function of IIR Notch filter ($\hat{H}(z)$) as shown in Eq. (7) in implementation of the floating point IIR Notch Filter on FPGA. First, we need to transform this transfer function, which is in Z-domain into new form, the difference equation, by using the property of Z-transform shown in Eq. (9).

$$y(n) = b_0 x(n) - 2b_0 \cos\omega_n x(n-1) + b_0 x(n-2) + 2r\cos\omega_n y(n-1) - r^2 y(n-2)$$

The output $y(n)$ in Eq. (9) requires many sign fixed mathematical processes such as sign fixed adder, sign fixed multiplier, and sign fixed shift. Therefore, we choose the Altera’s APEX DSP Development board (FPGA board) which contains sign fixed 10 Bit A/D and D/A. The architecture of floating point 32 Bit [6, 7] calculation in Altera’s APEX is shown in Fig. 3.

From Fig. 3, the processing system of this designed FPGA is divided into 4 main parts that are:

1. Sign fix point to floating point converter
2. Floating point multiplier
3. Floating point addition
4. Floating point to sing fix point converter

which contain details as shown in Figs. 4 ~ 7.

### 4. RESULT

In experiments, we set the values of the bandwidth of IIR Notch filter as 1 Hz and 2 Hz consecutively, and set the notch frequency at 50 Hz with sampling frequency of 5 kHz. With these assignments, we get the Frequency response graph as shown in Figs. 10 ~ 11. These frequency response graphs measured and represented by the Dynamic signal analyzer HP-35670 are really symmetric with high amplifications. These results are quite similar to the frequency response in Figs. 8 ~ 9 which are simulated by Matlab.
5. CONCLUSION

The FPGA notch filter designed in this paper is able to produce very high precision and accuracy frequency response between 1 Hz - 5 MHz, compared to the Magnitude response and Phase response simulated by Matlab. The filtering property of this FPGA is also function in the very narrow bandwidth (≥ 1 Hz) because of its 32-bit floating-point unit architecture. Unlike the software filter, this hardware filter also works fast and stable even in threatening environment. This stable and speedy function of hardware filter should be necessary in the elimination of sharp noise from AC power line which is frequently found in medical equipment.

REFERENCES


Fig. 8.1 Magnitude Response simulated by Matlab.

Fig. 8.2 Phase Response simulated by Matlab.

Fig. 9.1 Magnitude Response simulated by Matlab.

Fig. 9.2 Phase Response simulated by Matlab.

Fig. 10.1 Magnitude Response measured by Dynamic signal analyzer.

Fig. 10.2 Phase Response measured by Dynamic signal analyzer.

Fig. 11.1 Magnitude Response measured by Dynamic signal analyzer.

Fig. 11.2 Phase Response measured by Dynamic signal analyzer.