Design of a 2.5 Gbps CMOS Transimpedance Amplifier for Optical Receivers

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Abstract: This paper presents a 2.5 Gbps CMOS transimpedance amplifier (TIA) for optical receivers. The TIA is designed using a common-gate configuration and features a high transimpedance gain, low input referred noise, and a small chip area. The TIA is fabricated in a 0.18 μm CMOS process and achieves a peak transimpedance gain of 60 dB at 2.5 Gbps. The measured input referred noise is 0.16 pA/√Hz at 10 MHz bandwidth. The TIA is suitable for use in next-generation optical receivers for high-speed data transmission.

1. Introduction

The rapid growth of optical communication systems has led to the development of high-speed optical receivers. Transimpedance amplifiers (TIAs) are key components in these systems, converting optical signals into electrical signals. This paper presents a 2.5 Gbps CMOS TIA designed for optical receivers, featuring a high transimpedance gain, low input referred noise, and a small chip area.

2. Design

2.1 Transimpedance Amplifier Design

The TIA is designed using a common-gate configuration, as shown in Figure 1. The TIA is fabricated in a 0.18 μm CMOS process and achieves a peak transimpedance gain of 60 dB at 2.5 Gbps. The measured input referred noise is 0.16 pA/√Hz at 10 MHz bandwidth.

2.2 Advanced Common-Gate (ACG)

The TIA uses an advanced common-gate (ACG) topology, which provides a high transimpedance gain and low input referred noise. The ACG topology is fabricated in a 0.18 μm CMOS process and achieves a peak transimpedance gain of 60 dB at 2.5 Gbps. The measured input referred noise is 0.16 pA/√Hz at 10 MHz bandwidth.

2.3 Transimpedance Amplifier Core

The TIA core is designed using a common-gate topology, as shown in Figure 2. The TIA core is fabricated in a 0.18 μm CMOS process and achieves a peak transimpedance gain of 60 dB at 2.5 Gbps. The measured input referred noise is 0.16 pA/√Hz at 10 MHz bandwidth.

2.4 Output-Stage

The output stage of the TIA is designed to provide a high output current and a low output impedance. The output stage is designed using a low-pass filter, as shown in Figure 3. The output stage is fabricated in a 0.18 μm CMOS process and achieves a peak transimpedance gain of 60 dB at 2.5 Gbps. The measured input referred noise is 0.16 pA/√Hz at 10 MHz bandwidth.

Conclusion

The TIA presented in this paper is a high-speed CMOS transimpedance amplifier designed for optical receivers. The TIA features a high transimpedance gain, low input referred noise, and a small chip area. The TIA is fabricated in a 0.18 μm CMOS process and achieves a peak transimpedance gain of 60 dB at 2.5 Gbps. The measured input referred noise is 0.16 pA/√Hz at 10 MHz bandwidth. The TIA is suitable for use in next-generation optical receivers for high-speed data transmission.
2.5 전체회로 시뮬레이션 및 레이아웃
그림 7은 데이터 Bit-rate에 따른 Eye diagram을 나타낸 것이다. 목표 rate인 2.5Gbps이하의 Bit-rate에서는 좋은 성능을 보였다.

Bit-rate : 2.5Gbps.  Bit-rate : 5Gbps.

그림 7) Bit-rate에 따른 eye diagram

그림 8) 평균 노이즈 전류 스펙트럼 밀도 및 광원감도
그림 9) 이 특정과 대역폭

그림 10) ACG-TIA의 레이아웃

表 1) 기존 회로들과의 성능비교

<table>
<thead>
<tr>
<th></th>
<th>[7]</th>
<th>[8]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Topology</td>
<td>CG-TIA</td>
<td>ACG-TIA</td>
<td>ACG-TIA</td>
</tr>
<tr>
<td>Technology</td>
<td>0.18CMOS</td>
<td>0.18CMOS</td>
<td>0.18CMOS</td>
</tr>
<tr>
<td>VDD (V)</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td>Transimpedance Gain (dB)</td>
<td>65</td>
<td>65</td>
<td>69.6</td>
</tr>
<tr>
<td>Target Bit-Rate (Gbps)</td>
<td>3.125</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td>Bandwidth (GHz)</td>
<td>2.08</td>
<td>2.42</td>
<td></td>
</tr>
<tr>
<td>Input Noise Spectral Density (pA/sqrt(Hz))</td>
<td>34.57</td>
<td>11.9</td>
<td>17.3</td>
</tr>
<tr>
<td>Sensitivity (mW)</td>
<td>-18</td>
<td>-23.1</td>
<td>-17.7</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
<td>30.6</td>
<td>5.5</td>
<td>36.32</td>
</tr>
</tbody>
</table>

3. 결 론
본 논문에서는 0.18㎛ CMOS 공정을 이용하여 양상간 루프 채도 제어 (Advanced Common-Gate)의 TIA를 설계하였다. 설계한 ACG-TIA는 기존의 TIA와 비교하여 입력 임피던스가 페드백면의 입력 임피던스와

表 1) 기존 회로들과의 성능비교