GCC based Compiler Construction for Compact DSP32

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Abstract

Very Long Instruction Word (VLIW) executes multiple instructions in parallel. In order to exploit higher performance, i.e., higher parallelism, VLIW compiler groups as many instructions into one word as possible. In this paper, we show how to construct a VLIW C compiler based on GCC for CDSP32 (Compact Digital Signal Processor 32-bit) which is an embedded DSP processor to issue two instructions in one VLIW. Also, we evaluated the compiler on EEMBC benchmark; the experiment result showed that the total number of dynamic instructions of the VLIW compiler was reduced by 18% on average over without VLIW instruction scheduling.

1. Introduction

A hardware performance in modern embedded processor design is one of the most important issues because signal processing power becomes critical concern in multimedia devices. To achieve higher performance, many chip vendors have adopted hardware techniques to their own processors. Especially, the VLIW architecture [1] is an attractive solution in embedded processor design, because the VLIW architecture takes advantage of instruction level parallelism (ILP) in applications to execute instructions in parallel. Nevertheless, the VLIW architecture does not need complex hardware to schedule instructions, since the compiler provides VLIW instructions that is already scheduled considering ILP.

ZARAM [2] recently developed a 32-bit Compact DSP processor that supports the VLIW execution. The CDSP32 processor can execute two independent instructions at the same time. In this paper, we port GNU C Compiler [3] to the CDSP32 processor and apply an algorithm of VLIW instruction constructing. We also evaluate our work with EEMBC benchmark on the CDSP32 simulator and measure the total number of dynamic instructions. As a result, we could achieve 18% of performance enhancement in terms of the total number of dynamic instructions over without VLIW approach.

The rest of this paper is organized as follows. Section 2 explains the compiler construction for CDSP32. Section 3 discusses the VLIW constructing algorithm in detail. We show performance results in Section 4 and conclude this paper in Section 5.

2. Compiler Construction for CDSP32

The CDSP32 processor is a 32-bit DSP core capable of operating at 250MHz speed. It uses 16kB 4-way set-associative data/instruction caches and supports 8, 16, 32, 64-bit data size. The CDSP32 processor has 14 general-purpose registers, each of 32 bit width and two instruction issue logics for VLIW.

The CDSP32 processor supports arithmetic, logical, memory load/store, branch, and move operations. For GCC-based compiler construction, all the possible operations should be described as GCC IR (Intermediate Representation) in the compiler’s MD (Machine Description) file. In addition, all of logical registers should be defined as register classes according to their usages. The register classes are used as a constraint in the patterns.

Figure 1 illustrates an example of a single integer move pattern in the MD file. The GCC emits assembler mnemonics according to the constraint of operands. In Figure 1, we assigned mov op-code to register-to-register copy, and ld32 op-code to the case of memory-to-register load. Also, we added two attributes to each instruction; pattern type and VLIW information. The pattern type describes the kind of corresponding instruction, and the VLIW information explains which slot the instruction can go; slot0 or slot1. The VLIW constructing algorithm will be explained in the next section.

```
// Single Integer MOVE Pattern

#define _insn "mov\*"

@1
(match.operand:Si 0 // Destination operand
   "nonimmediate.operand" "-r,r,r,r,r,n")
@2
(match.operand:Si 1 // Source operand
   "general.operand" '"r,r,r,r,r,r")

0
mov $r0, $r1 // Register to Register copy
ld32 $a0, $r0 // Load from memory
ld $a0, $r1 // Assign immediate const to register
lrr $a0, $r1 // Register to SP register copy
store $a0, $x3, $x1 // Store to memory

悠_t["type", "mov, load, load, mov, store"]
悠_t["insn_type", "vliw,vliw,vliw,vliw,none,vliw"]
```

Figure 1. An example of a single integer move pattern in the MD file

3. Constructing VLIW Instruction

The CDSP32 processor can execute at most two instructions at a time by grouping them into a VLIW
instruction. However, several restrictions should be carefully handled to form the VLIW instruction: 1) one memory port is supported, two memory instructions cannot be grouped; 2) branch instructions such as jump and function call should be excluded; 3) instructions such as call, pop, and push should be put at the first slot of VLIW.

Before grouping instructions into a VLIW instruction, the compiler should check whether instructions can be executed in parallel. The GCC’s instruction scheduler checks the dependency. At each cycle, the scheduler provides a list of parallel instructions that can be executed together in one cycle. From the given list, the VLIW constructor chooses one or two instructions.

The detail of VLIW grouping can be explained as follow: 1) The CDSP32 compiler searches and identifies candidate instructions from the independent list to be put into slot0 and/or slot1 of VLIW. 2) The compiler tries to fill VLIW slots with the candidate instructions while considering the restriction rules of the CDSP32 processor; a pair of slot0 and slot1 instructions constructs one VLIW instruction. 3) The compiler marks the matching instructions into a linked list and reorders the instruction sequence if necessary: the instruction at slot0 must be put right before the instruction at slot1 in the independent list. At the end of a basic block scheduling, the CDSP32 compiler inserts a special instruction to mark the starting point of a VLIW in the RTL instruction sequence so that the CDSP32 processor can recognize them at run time. The VLIW constructing algorithm is as shown in Figure 2.

```c
/* list provided by GCC scheduler to identify instructions to execute within one cycle */
for each independent_insn_list {
  for each insn in independent_insn_list{
    // slot0, slot1 or none (cannot be used in VLIW)
    type = recognize_VLIW_type_of_insn(insn);
    new_vliw = findNothingVLIWInsn(type, independent_insn_list, insn);
    if(new_vliw){
      vliw_insn_list += new_vliw;
      reorder_DSP_insn(insn, new_vliw, independent_insn_list);
    }
  }
}
for each link in vliw_insn_list {
  // insert a vliw marker before slot0 DSP
  insert_vliw_marker(link);
}
```

Figure 2. Pseudo code of VLIW constructing algorithm.

Since the CDSP32 processor can execute only one VLIW instruction at a time, the algorithm exits the innermost loop after finding a VLIW instruction. Table 1 shows target HOOKs to enable the VLIW construction.

Table 1. Target HOOKs

<table>
<thead>
<tr>
<th>HOOK</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TARGET_SCHED_REORDER</td>
<td>Main VLIW instruction constructing</td>
</tr>
<tr>
<td>TARGET_SCHED_REORDER2</td>
<td>The order of instruction inside the list can be changed after GCC scheduler process, reorder the VLIW slots if necessary</td>
</tr>
<tr>
<td>TARGET_SCHED_FINISH</td>
<td>Insert marker instruction to mark VLIW groups</td>
</tr>
</tbody>
</table>

4. Performance Evaluation

Figure 3 shows an example of C and assembly codes when the VLIW constructing algorithm is applied. We can see two vliw instructions each of which are followed by two independent instructions. When the CDSP32 processor fetches a vliw instruction, the subsequent two instructions (i.e. rdr, ld) are grouped into a VLIW instruction and executed in parallel.

For our performance evaluation (in terms of the number of dynamic instructions), we used EEMBC benchmarks [4] on the CDSP32 simulator. Figure 4 shows the number of dynamic instructions on non-vliw and vliw compiler. The non-vliw and vliw indicate versions before and after applying the VLIW constructing algorithm, respectively. The result was normalized to the number of dynamic instructions of the non-vliw. We could reduce the number of dynamic instructions by 18% on average in the vliw.

Figure 5 shows the ratio of instructions combined into VLIW instructions among total instructions. We could match the VLIW instructions about 36% on average. This result represents that our VLIW constructing algorithm is working well despite the processor’s hardware restrictions.

```c
inf sum=0;
inf main(void) {
  int i;
  for (i=0; i < 10; ++i) {
    sum += i;
    i;
  }
  return sum;
}
```

```c
main:
  #r1 r7
  pushx 0x802
  vliw
  rdr r7, sp
  ld r1, sum
  ld r2, r1, r1
  add r0, r1, 55
  vliw
  ld r1, sum
  mov r0, r8
  st r32, r1, r8
  #r7 r1
  popx 0x802
  ret UNK
```

Figure 3. Example of C and assembly codes.

5. Conclusion

The VLIW architecture is a popular solution for high performance DSP processor, because it can execute multiple instructions in parallel without complex hardware. However, the compiler has to determine the VLIW instructions that can be run in parallel. In order to achieve good performance, the compiler has to schedule instructions well to take advantage of as much ILP as possible.
In this paper, we built the Compact DSP32 compiler based on GCC, and applied VLIW constructing algorithm for supporting VLIW instructions. Compared to the non-vliw, the vliw reduced the number of dynamic instructions by about 18% on average for EEMBC benchmarks. In addition, we could extract the VLIW instructions about 36% on average.

References