A New Design-for-Testability Circuit for Low Noise Amplifiers

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Abstract

This paper presents a new Design-for-Testability (DfT) circuit for 4.5-5.5GHz low noise amplifiers (LNAs). The DfT circuit measures gain, noise figure, input impedance, input return loss, and output signal-to-noise ratio for the LNA without external expensive equipment. The DfT circuit is designed using 0.18μm SiGe technology. The circuit utilizes input impedance matching and DC output voltage measurements. The technique is simple and inexpensive.

Keywords: DfT circuit, LNA, RFIC Chip

I. Introduction

Rapid growth in system integration of RFIC chips for wireless communications is overwhelming. The integration density and complexity of these devices increase with consumer demands in functionality. With test cost of 40% of the total production cost, a low cost way to test RFIC chips is an important aspect. In spite of the considerable research underway to reduce the test overhead in RFIC chips[1-7], the difficulties in testing still remain to be the major tackle of the product manufacturing. The problems come from the

limited access to major components of the internal RF structures and the non-linear effects in RF faults may cause on a circuit under test[8-9]. To solve these problems, the Built-In Self-Test (BIST) technique using Design-for-Testability (DfT) in the RF and mixed signal domain is applied as a suitable test approach on the chip[1-6]. Especially research for possible strategies to implement RF DfT for the RF chips has been performed[13-8], but a suitable solution still remains as a bottleneck.

In this paper, a low-cost testing of 4.5-5.5GHz low noise amplifier (LNA) using a new RF DfT circuit for measuring gain, noise figure, input impedance, input return loss, and output signal-to-noise ratio is presented. The test technique utilizes input impedance matching and output transient voltage measurements. The LNA and DfT circuits are integrated on a single chip using 0.18μm SiGe technology. This test technique requires only the use of DC meter and RF voltage
source generator.

II. Test Set-up and Approach

Traditional way of testing LNA involves measurements of S-parameter, noise figures, SNR and IIP3 using variety of different RF test equipment. Our proposed DfT technique utilizes on-chip BIST circuit to measure important LNA specifications without major external test equipment.

Figure 1 shows proposed test set-up which measures gain, noise figure, input impedance, input return loss, and output signal-to-noise ratio for the LNA. The on-chip RF DfT circuit consists of test amplifier (TA) and two RF peak detectors (PD1 and PD2). The RF peak detectors are used to convert RF signal to dc voltage\(^{[2]}\). The complete LNA test structure consists of the RF voltage source generator \((V_{\text{in}})\), LNA chip with RF DfT circuit, DC meter, 50 ohm load impedance \((Z_{\text{L}})\), and three external switches \((S_1, S_2\) and \(S_3)\).

Figure 2 shows real measurement set-up for measuring gain, noise figure, input impedance, input return loss, and output signal-to-noise ratio of the LNA. The measurement set-up contains a SMA connector for input of RF signal voltage source generator \((V_{\text{in}})\), a SMA connector for 50 ohm load impedance \((Z_{\text{L}})\) matching, two SMA connectors for two outputs \((V_{\text{T1}}\) and \(V_{\text{T2}})\), three low loss RF relays and RF on-chip. The input transmission matching is considered between LNA and TA circuits. The positions of the relays are controlled to measure the output DC voltages, \(V_{\text{T1}}\) and \(V_{\text{T2}}\) through the DfT circuit. These relays are controlled by DeMux chip on an external evaluation board.

In our testing approach, we assumed a unilateral LNA where the reverse isolation \((S_{\text{II}})\) is zero. However, a real unilateral LNA has the maximum error of less than +/-0.005dB at 4.5-5.5GHz as discussed in [10]. In this paper, we consider measurements of input impedance, gain, noise figure, input return loss, and output signal-to-noise ratio. The following sections describe test details of these parameters.

A. Input Impedance

Figure 3 shows the equivalent circuit for the inputs of the LNA and test amplifier.

\(Z_1\) and \(Z_2\) represent the input impedance of the LNA and test amplifier, respectively. These impedances have real and imaginary parts. The input impedance measurement is performed with the switches \(S_2\) and \(S_3\) in closed position and the switch \(S_1\) in open position. The overall test technique is to find any deviations between the source impedance...
(Rs) and the input impedances (Z1 and Z2). For example, the TA of Figure 1 looks for changes in input impedance of the LNA for any mismatch with the source resistance. In case of a mismatch due to a defect or a process variation, the transient dc voltage of the PD2 is presented at the test output in dc measurement.

**Case I: Fault-Free LNA**

We consider fault-free LNA with good input matching condition. The Equation (1.1) represents the theoretical values for the voltage across the input impedances of the LNA and TA. The TA is designed with the input and output matching impedances of 50, and a flat gain of G2≈3 to increase test output voltage to the original input voltage level \(|v_m|\) as indicated in Equation (1.2). The DFT circuit monitors the transient dc voltage \(V_{T2}\) as shown in Figure 1. Equations (1.1) and (1.2) represent important expressions that are developed to derive input impedance of the LNA.

\[
|v'_1| = \left| \frac{Z_1/Z_2}{[R_1 + (Z_1/Z_2)]} \right| v_m = \left| \frac{Z_1}{2Z_1 + R_1} \right| v_m
\]

\[
V_{T2} = v_{in} + V_{02} = |v_1| \times (G_2 \approx 3) + V_{02}
\]

\[
= \left| \frac{Z_1}{2Z_1 + R_1} \right| v_m \times (G_2 \approx 3) + V_{02}
\]

(1.1)

(1.2)

where \(|Z_1|\) and \(|Z_2|\) are magnitudes of input impedances of LNA and TA, respectively, \(G_2\) is voltage gain of TA and \(V_{02}\) is dc output voltage of the peak detector, PD2. Since the complex impedances of the LNA and the test amplifier can be said to have Re\((Z_1)\) >> Im\((Z_1)\) and Re\((Z_2)\) >> Im\((Z_2)\) with good input impedance matching at the frequency operation range of 5-5.25GHz, their magnitudes \(|Z_1|\) and \(|Z_2|\) are respectively expressed by

\[
|Z_1| = \sqrt{[\text{Re}(Z_1)]^2 + [\text{Im}(Z_1)]^2} \approx \text{Re}(Z_1)
\]

\[
|Z_2| = \sqrt{[\text{Re}(Z_2)]^2 + [\text{Im}(Z_2)]^2} \approx \text{Re}(Z_2)
\]

(1.3)

(1.4)

From Equations (1.1) to (1.4), we can express the new magnitude of input impedance of LNA as

\[
|Z_1| = R_s \frac{K_1}{1 - 2K_1} [\Omega]
\]

(2.1)

where \(K_1 = G_{02} / G_2\) and \(G_{02}\) is the voltage gain obtained by the input matching test.

\[
G_{02} = \frac{V_{T2} - V_{02}}{|v_m|}
\]

(2.2)

**Case II: Faulty LNA**

The LNA can have catastrophic faults such as resistive short and open faults due to the spot defects, and parametric faults such as unusual parameter variations and unusual process variations\(^{[4,8-9]}\). In this case, there is a certain variation in magnitude of input impedance of LNA because of change in its input matching condition. Under a faulty case, Equation (2.1) can be expressed as Equation (3). \(\overline{V}_{T2}\) replaces \(V_{T2}\) under a faulty case.

\[
|Z_1| = R_s \frac{\overline{K}_1}{1 - 2\overline{K}_1} [\Omega]
\]

(3)

where \(|\overline{Z}_1|\) represents \(|Z_1|\) under a faulty case,

\[
\overline{K}_1 = \frac{G_{02}}{G_2}, \quad \overline{G}_{02} = \frac{\overline{V}_{T2} - \overline{V}_{02}}{|v_m|}
\]

Consider input impedance of the LNA obtained by DFT at between 4.5GHz and 5GHz, and 5.25GHz and 5.5GHz. In this case, there are certain variations in magnitudes of input impedance of both LNA and test amplifier because of changes in their input matching.
condition. The test amplifier was designed by less than 10\% magnitude variation of input impedance as compared to magnitude of input impedance at the operation frequency range of 5-5.25 GHz. When this approximation is applied, \( |Z_2| \approx \text{Re}(Z_2) \) for \( \text{Re}(Z_2) \gg \text{Im}(Z_2) \). Thus, we derive Equation (4) at between 4.5 GHz and 5 GHz, and 5.25 GHz and 5.5 GHz.

\[
|Z_1| = \frac{R_s}{1 + \left( \frac{R_s}{|Z_1|} \right) G_{02} / G_2} \cdot \frac{G_{02}}{G_2} \cdot \frac{G_2}{G_2 + \Delta G_2} \cdot |Z_1| \Delta \quad \Omega \tag{4}
\]

where \( \Delta G_2 \) is voltage gain variation of test amplifier, and \( \Delta |Z_1| \) is magnitude variation of input impedance of test amplifier.

**B. Voltage Gain**

**Case I: Fault-Free LNA**

The voltage gain measurement is performed with the switch S1 in closed position and the switches S2 and S3 in open position from Figure 1. The voltage gain measurement is based on monitoring transient dc voltage of the first peak detector, PDI. The DfT monitors the transient dc voltage \( V_{TI} \) as shown in Figure 1.

\[
V_{TI} = G_1 |V_L| + V_{01} \tag{5}
\]

where \( V_{01} \) is dc output voltage of PDI.

From Figure 1, we obtain Equation (6).

\[
|V_L| = \frac{|Z_1|}{R_s + |Z_1|} |V_{in}| \tag{6}
\]

Therefore, from Equations (5) and (6), we get voltage gain of the LNA using the BIST:

\[
G_1 = \frac{V_{TI} - V_{01}}{|V_L|} = \left( 1 + \frac{R_s}{|Z_1|} \right) G_{01} \tag{7}
\]

where \( G_{01} \) is voltage gain measured by gain test.

\[
G_{01} = \frac{V_{TI} - V_{01}}{|V_{in}|}
\]

**Case II: Faulty LNA**

Under a faulty case, Equation (7) can be expressed to Equation (8).

\[
\overline{G_1} = \left( 1 + \frac{R_s}{|Z_1|} \right) \overline{G_{01}} \tag{8}
\]

where

\[
\overline{G_{01}} = \frac{V_{TI} - V_{01}}{|V_{in}|}
\]

**C. Noise Figure**

The conventional formula for noise figure follows:

\[
NF = 1 + \frac{N_2}{G_1 N_1} \tag{9}
\]

where \( G \) is amplifier power gain, \( N_1 \) is the LNA source resistance noise power, and \( N_2 \) is the inherent output noise.

**Case I: Fault-Free LNA**

If there is no defect or acceptable process variation from input impedance and voltage gain measurements, the noise figure obtained by DfT can be expressed using noise figure required by LNA specification.

\[
NF = 1 + \frac{G_2}{G_1} (N_2 - 1) = 1 + \frac{|Z_1|}{[R_s + |Z_1|]} G_2 \left( \frac{G_2}{G_1} (N_2 - 1) \right) \tag{10}
\]
where $G_0$ and $NF_0$ are power gain and noise figure required by the specification, respectively.

**Case II: Faulty LNA**

Under the case of fault, Equation (10) can be expressed as Equation (11).

$$\overline{NF} = 1 + \left( \frac{|Z_1|}{[R_s + |Z_1|]} \right)^2 \cdot \frac{G_0}{G_{01}} (NF_0 - 1)$$

**D. Input Return Loss**

**Case I: Fault-Free LNA**

The input return loss ($RL_{in}$) is also important parameter in LNA. Using unilateral assumption\textsuperscript{[10-11]}, we get input return loss of the LNA using the BIST.

$$RL_{in} = 20 \log \left( \frac{|Z_1 - Z_0|}{|Z_1 + Z_0|} \right) = 20 \log \left( \frac{|Z_1 - Z_0|}{|Z_1| + Z_0} \right)$$

**Case II: Faulty LNA**

Under a faulty case, Equation (12) can be expressed as Equation (13).

$$\overline{RL}_{in} = 20 \log \left( \frac{|Z_1 - Z_0|}{|Z_1| + Z_0} \right)$$

**E. Output Signal-to-Noise Ratio**

Noise figure has been defined in a number of different ways. The most commonly accepted definition\textsuperscript{[10-11]} is

$$NF = \frac{SNR_{in}}{SNR_{out}}$$

where $SNR_{in}$ and $SNR_{out}$ are the signal-to-

**Case I: Fault-Free LNA**

Using open literature [10-11] and Figure 1, the $SNR_{in}$ measured at the input can be expressed as Equation (15).

$$SNR_{in} = \left( \frac{|Z_1|V_{in}^2}{(R_s + |Z_1|)^2} \right) \cdot \frac{R_s}{R_s + |Z_1|} \left( \frac{kT}{4} \right)$$

where $kT$ is -204 dB/Hz and $B$ is signal bandwidth. From Equations (10) and (14) to (15), we get the $SNR_{out}$ at the output using DfT.

$$SNR_{out} = \frac{SNR_{in}}{R_s} \cdot \left( \frac{R_s + |Z_1|}{kT} \right) \cdot \frac{1}{NF}$$

**Case II: Faulty LNA**

Under the case of a fault, Equation (16) can be expressed as Equation (17).

$$SNR_{out} = \frac{SNR_{in}}{R_s} \left( \frac{R_s + |Z_1|}{kT} \right) \cdot \frac{1}{NF}$$

**III. Fault Models**

Both catastrophic faults and parametric faults are considered for BJTs and passive components\textsuperscript{[11]} . Spot defects that can severely degrade the performance or result in chip malfunction are considered\textsuperscript{[10]} . We used 0.18μm BICMOS technology, however, only defects in Bipolar Junction Transistors are considered since the LNA is designed with BJTs. Resistor and inductor with open faults are selected to have approximately 10 times the given values, and resistor and inductor with short faults are selected to have approximately 0.1 times the given values. For a capacitor, open
faults have approximately 0.1 times of the given value, and short faults have approximately 10 times of the given value\textsuperscript{[1]}. We considered ±10% to ±50% variations in resistors, capacitors and inductors, and ±25% and ±50% for number of emitters, emitter width and length variations in BJTs for parametric faults. A total of 173 different fault models are considered. Amongst them are a fault-free model, 28 different catastrophic fault models and 144 different parametric fault models.

In addition to inserting catastrophic faults into the simulations, we also performed Monte Carlo simulations and sensitivity analysis. Monte Carlo analysis is performed to ensure that no parametric faults can mask catastrophic faults. If the range of response of a catastrophic faulty circuit is indiscernible from the fault-free case, then the parametric fault will mask the catastrophic fault. We have considered variable process parameters such as surface mobility, junction depth, substrate doping, cut-off voltage, transistor emitter lengths, and transistor emitter widths for Monte Carlo analysis. Each of the device model parameters listed above was randomly perturbed with a Gaussian distribution from one simulation to the next. The distribution of the Gaussian random variables was selected at 10% of nominal at 30.

IV. LNA and DfT Circuit Analysis

The two-stage LNA is designed and its schematic is shown in Figure 4. It is designed for 5GHz 802.11a wireless LAN application. It is powered by a 1 volt supply. The complete design consists of four HBT transistors, five inductors, five capacitors and six resistors, all on a single chip.

The proposed DfT circuit is shown in Figure 5. It consists of test amplifier (TA) and peak detector (PD2) circuit stages. The other peak detector circuit (PD1) is also a part of the BIST circuit and it has the same topology as the PD2 circuit as shown in Figure 5. The bias stage utilizes band-gap reference circuit for a low supply voltage and low power dissipation.

그림 4. 5GHz 저잡음 증폭기 회로도

Fig. 4. Schematic diagram of 5GHz LNA.

The inductor (\(L_{\text{G}}\)) is used for input and output impedances matching. The RF peak detectors are used to convert RF signal to DC voltage\textsuperscript{[12]}. The bias resistors (\(R_{\text{G}}\) and \(R_{\text{B}}\)) shown in Figure 5 are used to keep transistor Q\textsubscript{M} in the active region so that the transistor acts as a rectifier. The diode connections have advantages of resulting in keeping the base-collector junction at zero bias. The smallest amount of minority charge storage during forward biased condition will be highly beneficial to rectification of RF signals\textsuperscript{[11]}. To reduce the output ripple voltage, \(R_{\text{G}}\) and \(C_{\text{G}}\) are chosen with large values.

We processed a total of 173 defect cases which resulted in chip layouts of 173 times for post processing of defects. We used Cadence to perform layouts and post processing. However, we typically fabricated a total of 10 cases including defect-free and 9 defect cases. Figure 6 illustrates the chip micrograph of the LNA with DfT circuit. As an example, a

그림 5. 검사용 설계 회로도

Fig. 5. Schematic diagram of DfT.
defective capacitor can be put into the circuit schematic of Figure 4 and Cadence will automatically do a layout of the capacitor. This process has been performed for all 173 cases and a post processing has been done for each to verify the true values of parasitics. We used the values that were extracted from the layout to perform circuit simulation. It was observed that the physical size of each circuit element on the chip layout varied with respect to the values given in the schematic. The physical chip area is approximately 1.45mm×1.45 mm using the 0.18μm BiCMOS SiGe process.

V. Results

1. Defects vs. Outputs

Figures 7(a) and (b) show the scatter plots of transient DC voltages for various faults including open and short and parametric variations in low noise amplifier. The fault–free LNA provided voltages of 180mV and 445mV for $V_{T2}$ and $V_{T1}$, respectively. As can be seen from Figure 7(a), most of the catastrophic faults are in the lower end of $V_{T1}$ with varying $V_{T2}$. For resistor and transistor faults shown in Figure 7(a), the observed output voltages $V_{T1}$ remain in far left side as compared to a fault–free value. This result reveals that lower voltages of $V_{T1}$ indicate faults in resistors and transistors. These results show that the proposed DfT structure is suitable to detect variety of faults.

Figure 7(b) shows the scatter plot for parametric variations. It shows that the parametric faults are concentrated near the fault–free case. These transient voltages ($V_{T1}$ and $V_{T2}$) are measured after 40 nanoseconds settling time of the peak detectors, PDI
Table 1. Measured \( V_{T1} \) and \( V_{T2} \) by DIT circuit.

<table>
<thead>
<tr>
<th>Test Voltage</th>
<th>( V_{T1} ) [mV]</th>
<th>( V_{T2} ) [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fault-free</td>
<td>445.0</td>
<td>180.0</td>
</tr>
<tr>
<td>Q1 Base Open</td>
<td>127.3</td>
<td>209.6</td>
</tr>
<tr>
<td>Q1 B-E Short</td>
<td>127.3</td>
<td>220.0</td>
</tr>
<tr>
<td>Q1 E-C Short</td>
<td>155.2</td>
<td>144.6</td>
</tr>
<tr>
<td>( L_b + 30% )</td>
<td>389.3</td>
<td>194.8</td>
</tr>
<tr>
<td>( L_b + 40% )</td>
<td>383.5</td>
<td>192.0</td>
</tr>
<tr>
<td>( L_b + 50% )</td>
<td>375.8</td>
<td>189.8</td>
</tr>
</tbody>
</table>

and PD2 to ensure steady-state DC value. The output RC time constant of the peak detector contributed to the settling time constant.

We used RF input source of 100mV to 180mV at 4.5-5.5GHz. The DC voltages \( V_{T1} \) and \( V_{T2} \) are measured using a conventional DC meter.

Table 1 shows partial list of actual \( V_{T1} \) and \( V_{T2} \) values for several faults of results shown in Figure 7. These results are measured at 5.25GHz. In this table, we considered faults in transistor Q1 and inductor \( L_b \). These results are used to obtain voltage gains, noise figures and magnitudes of input impedances of the LNA. As shown in Table 1, fault-free value was significantly different from faulty values.

Using the values shown in Table 1, Table 2 lists partial values of input impedances, gains, noise figures, input return losses and output signal-to-noise ratios. For a good input matching, the LNA must have input impedance of \( Re(Z1) \approx 50 \) \( \Omega \) and \( Im(Z1) \approx 0 \), however, the designed LNA showed acceptable tolerance of \( Re(Z1) \approx 45 \pm 10 \Omega \) from the process variation. As shown in Table 2, for fault-free case, the proposed DIT showed very small error of 4% in input impedance, gain, noise figure, input return loss and output signal-to-noise ratio compared to external equipment test. External equipment test includes using expensive RF test equipment.

These results reveal that our proposed on-chip DIT scheme is suitable for functional test of the LNA. Using the RF Spectre suite of tools in Cadence, we were able to simulate the conventional testing. We noticed that conventional testing provided significant differences between fault-free and faulty LNA. On the other hand, the proposed DIT provided with a similar differences between the two. Therefore, the proposed DIT structure provided the same fault coverage with significantly less cost. The fault detection of the LNA can be made by looking at the gain, \( NF \), impedance, input return loss or output signal-to-noise ratio variations. The decreased inductance values did not vary much from the fault-free value. Therefore, we did not list them in Table 2.

The proposed on-chip DIT scheme showed fault coverage of 100% for catastrophic faults and 89% for process variations. There was very small deviation between the conventional and proposed on-chip DIT scheme for fault-free case as indicated in Table 2.

2. Frequency vs. Outputs

Table 3 lists gain and input impedance of test amplifier. These results are used to obtain magnitudes of input impedances of the LNA as shown in Equation (4). Because the test amplifier is designed with \( Re(Z_2) \gg Im(Z_2) \) at the frequency between 4.5GHz and 5.5GHz, phase shift for input impedance of test
Table 3. Gains and input impedances of test amplifier.

<table>
<thead>
<tr>
<th>Frequency [GHz]</th>
<th>S-parameter Results</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$G_2 \pm \Delta G_2$</td>
</tr>
<tr>
<td>4.50</td>
<td>2.80</td>
</tr>
<tr>
<td>4.75</td>
<td>2.92</td>
</tr>
<tr>
<td>5.00</td>
<td>3.10</td>
</tr>
<tr>
<td>5.25</td>
<td>3.06</td>
</tr>
<tr>
<td>5.50</td>
<td>2.98</td>
</tr>
</tbody>
</table>

Table 4. Measured $V_{T1}$ and $V_{T2}$ by DIT circuit.

<table>
<thead>
<tr>
<th>Frequency [GHz]</th>
<th>$V_{T1}$ [mV]</th>
<th>$V_{T2}$ [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.50</td>
<td>400</td>
<td>166.2</td>
</tr>
<tr>
<td>4.75</td>
<td>421</td>
<td>160.3</td>
</tr>
<tr>
<td>5.00</td>
<td>448</td>
<td>171.4</td>
</tr>
<tr>
<td>5.25</td>
<td>445</td>
<td>180.0</td>
</tr>
<tr>
<td>5.50</td>
<td>432</td>
<td>189.0</td>
</tr>
</tbody>
</table>

Table 5. Compared results of external equipment test and proposed on-chip DIT circuit.

<table>
<thead>
<tr>
<th>Frequency [GHz]</th>
<th>External Equipment Test</th>
<th>Proposed On-Chip DIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.50</td>
<td>16.40</td>
<td>38.45</td>
</tr>
<tr>
<td>4.75</td>
<td>17.76</td>
<td>33.08</td>
</tr>
<tr>
<td>5.00</td>
<td>17.95</td>
<td>32.57</td>
</tr>
<tr>
<td>5.25</td>
<td>17.16</td>
<td>40.27</td>
</tr>
<tr>
<td>5.50</td>
<td>15.96</td>
<td>55.24</td>
</tr>
</tbody>
</table>

amplifier at this frequency range can be neglected.

Table 4 lists $V_{T1}$ and $V_{T2}$ measured by DIT circuit as a function of frequency. These results are also used to obtain voltage gains and magnitudes of input impedances of the LNA as shown in Equations (2.1) and (7). As we can expect from these results, $V_{T1}$ has higher values at the operation frequency, and when the frequency is increased, $V_{T2}$ is also increased.

The compared results of external equipment test and proposed on-chip DIT for good LNA as a function of frequency are listed in Table 5. Our proposed DIT results also showed good approximation results compared to external equipment test.

VI. Conclusions

This paper proposed a new low-cost Design-for-Testability (DFT) circuit for measuring gain, noise figure, input impedance, input return loss and output signal-to-noise ratio of 4.5-5.5GHz LNA. Our DIT scheme utilized input impedance and DC output voltage measurements. The LNA and DIT circuits were designed using 0.18μm BiCMOS SiGe technology. The DIT circuit consisted of test amplifier and two RF peak detectors. This technique requires only use of common DC meters and RF voltage source generator. We believe that proposed DIT technique is simple and inexpensive.

References


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