GaAs on Si substrate with dislocation filter layers for wafer-scale integration

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Abstract
GaAs on Si grown via metalorganic chemical vapor deposition is demonstrated using various Si substrate thicknesses and three types of dislocation filter layers (DFLs). The bowing was used to measure wafer-scale characteristics. The surface morphology and electron channeling contrast imaging (ECCI) were used to analyze the material quality of GaAs films. Only 3-μm bowing was observed using the 725-μm-thick Si substrate. The bowing shows similar levels among the samples with DFLs, indicating that the Si substrate thickness mostly determines the bowing. According to the surface morphology and ECCI results, the compressive strained indium gallium arsenide/GaAs DFLs show an atomically flat surface with a root mean square value of 1.288 nm and minimum threading dislocation density (TDD) value of $2.4 \times 10^7$ cm$^{-2}$. For lattice-matched DFLs, the indium gallium phosphide/GaAs DFLs are more effective in reducing the TDD than aluminum gallium arsenide/GaAs DFLs. Finally, we found that the strained DFLs can block propagate TDD effectively. The strained DFLs on the 725-μm-thick Si substrate can be used for the large-scale integration of GaAs on Si with less bowing and low TDD.

Keywords
bowing, heteroepitaxy, metalorganic chemical vapor deposition, threading dislocation density

1 | INTRODUCTION

GaAs on Si substrates has been widely studied in heterostructure growth because of the need for large-area, low-cost, and monolithic integration of III–V optical devices with Si-integrated circuits in the field of photonic integrated circuits. Among the differences, the two main mismatches, namely, the lattice constant (4% difference) and thermal expansion coefficient (TEC) ($6.63 \times 10^{-6}$ K$^{-1}$ and $2.3 \times 10^{-6}$ K$^{-1}$ for GaAs and Si, respectively) between GaAs and Si, make growing a high-quality GaAs layer on a Si substrate challenging. These mismatches generate a large threading dislocation density (TDD) degrading device performance and causing severe bowing of the heteroepitaxial wafer and cracks in the GaAs film.
Several techniques have been used to reduce the TDD, including thermal cycling annealing (TCA) [1–3], two-step growth [4–8], and using dislocation filter layers (DFLs) [9–17]. TCA reverses the threading dislocation’s (TD’s) motion with the opposite direction of the Burgers vectors [1–3]. Moreover, the low-temperature growth of GaAs, the first stage of the two-step growth, improves crystallization by forming a seed layer on the Si substrate [4–8]. Superlattice layers, DFLs, inserted into the bulk of the GaAs layer also actively initiate annihilating TDs. These DFLs are composed of various materials, typically AlGaAs/GaAs [9,10], lattice-matched InGaP/GaAs [11–13], and strained InGaAs/GaAs [14–19]. Several studies have reported growing high-quality GaAs on Si using DFLs using molecular beam epitaxy (MBE) [14–17] and metalorganic chemical vapor deposition (MOCVD) [18,19] and assessed the crystal quality through analyses, such as examining the surface morphology, electron channeling contrast imaging (ECCI), photoluminescence, and testing unit device performance. However, no studies have measured the bowing of GaAs on Si using DFLs to assess the wafer-scale characteristics. Few papers have described the bowing and crack formation in GaAs on Si that was grown using the two-step growth and TCA methods [1,2].

Wafer bowing is attributed to the difference in the TECs of materials. Because the TEC of GaAs is much larger than that of Si, severe wafer bowing and tensile strain in GaAs occur after cooling from high growth temperature to room temperature in MOCVD. Severe wafer bowing impedes mass production in the lithography step using wafer steppers and causes difficulties in subsequent device-processing steps. Moreover, the residual strain in wafers can cause TDD and cracking, degrading device performance. Therefore, bowing measurement can also be used to monitor residual stress in wafers caused by thermal and mechanical effects during growth.

In this study, we systematically investigate GaAs on Si wafers by analyzing the bowing and crystal quality. Unlike other results of GaAs on Si where bowing depended on the thickness of the GaAs layer on the Si substrate [20,21] and composition of the InGaP layer [22], the thickness of the GaAs layer, herein, was fixed to 1.5 μm, and that of the Si substrate was varied from 270 μm to 750 μm. The optimum thickness of the Si wafer produces less bowing of GaAs on Si using both the experimental and calculation results. Furthermore, the wafer-scale characteristics and material properties of GaAs on Si using various DFLs were investigated via examining bowing, surface morphology analysis, and ECCI.

2 | EXPERIMENT

A GaAs layer was grown on 2-inch Si (100) substrates with a 4° miscut angle using MOCVD. In our MOCVD system, a vertical reactor with low pressure was used, and up to four 2-inch wafers can be used simultaneously to grow the III–V layer. Si wafers with thicknesses of 279 μm, 500 μm, and 725 μm were used to investigate the wafer bowing characteristics depending on the Si wafer thickness. Before the GaAs growth, the substrates were dipped in hydrofluoric acid, rinsed in deionized water, and heated to 900°C in a hydrogen- and arsine-rich atmosphere. The GaAs layers were grown using the two-step growth method, with an aluminum-arsenide initial seed layer [23], followed by TCA. TCA was conducted between 800°C and 350°C. After TCA, three sets of DFLs with a 300-nm GaAs spacer layer were used to reduce the TD that can arise from the thermal and lattice mismatch between GaAs and Si. Each sample had a different DFL composed of the most widely used materials, such as In0.5Ga0.5P/GaAs, Al0.45Ga0.55As/GaAs, and In0.1Ga0.9As/GaAs. Each DFL consisted of five superlattice repeats. The control sample without DFLs was also grown identically using the same growth conditions that were used for the samples with DFLs. To avoid crack formation, the total GaAs layer thickness was maintained at less than 2.5 μm because the critical thickness causing crack formation is between 2.9 μm and 3.9 μm [24].

Figure 1A,B shows a schematic of the growth method and the sample structure, respectively. The wafer-scale characteristics were evaluated by analyzing the bowing and crystal quality of the samples using Nomarski imaging, atomic force microscopy (AFM), and ECCI. The bowing characteristic was measured using PLATOM of EtaMax commercial manufactured equipment. In this equipment, bowing parameters were calculated by analyzing the Sori [25] using a laser displacement sensor. GaAs bowing on Si wafers with thicknesses of 279 μm, 500 μm, and 725 μm was also calculated using ANSYS software.

3 | RESULTS AND DISCUSSION

Figure 2A shows a bowing map of GaAs on a Si substrate. The bowing map shows the height across the wafer, which is the vertical distance from the wafer surface to the optical sensor in EtaMax. The maximum height is at the center, decreasing uniformly from the center to the outside of the wafer. Figure 2B shows the experimental and simulation results of wafer bowing according to the
thickness of the Si wafer. For simulating wafer bowing, Stoney’s equation was used to calculate the curvature without considering the lattice parameter. Stoney’s equation (1) is frequently used to determine the stress of a thin film.

\[
\sigma_{\text{th}} = \left[ \frac{E_f}{1 - \nu_f} \right] \times (\sigma_s - \sigma_f) \times (T_G - T_0) = \left[ \frac{E_f}{1 - \nu_f} \right] \times t_s^2 \left( \frac{6 \times t_f \times R}{C_0/C_1/C_2/C_3} \right) \tag{1}
\]

where \( E_f \) is Young’s modulus of GaAs \( (8.55 \times 10^{11} \, \text{dyn/cm}^2) \), \( \nu_f \) is Poisson’s ratio of GaAs \( (0.29) \), and \( \sigma_s \) and \( \sigma_f \) are the TECs of GaAs and Si, respectively. Here, \( T_G \) is the growth temperature, \( T_0 \) is the room temperature, \( R \) is the radius of curvature, and \( t_s \) and \( t_f \) are the thicknesses of the substrate and the thin film, respectively.

The experimental bowing and simulation correlated well. Less bowing was observed as the Si wafer thickness increased. This correlation confirms that the difference in TEC, rather than lattice mismatch, predominantly determines wafer bowing because the lattice constant parameter was not considered in the simulation. For a given 1.8-μm-thick GaAs film, the maximum bowing was 32 μm with the Si substrate thickness of 279 μm. However, the maximum bowing was only 3 μm with the Si substrate thickness of 725 μm. This 3-μm bowing is a small enough value for the practical use of the I-line stepper. To study the effect of DFLs, the bowing of GaAs on Si using various DFLs was also observed. Table 1 shows the maximum bowing value. The bowing of all samples with DFLs shows levels similar to that of the control sample because the DFL layers, which are thin (300 nm) compared with the total thickness of GaAs (1.8 μm), do not significantly affect the difference in TEC.

**FIGURE 1** (A) The schematic growth sequence of GaAs on Si with DFLs. (B) The structure of GaAs on Si with various types of DFLs

**FIGURE 2** (A) The bowing map of the control GaAs on the Si sample. (B) The experimental and calculated bowing along the x-axis on the wafers with thicknesses of 279 μm, 500 μm, and 725 μm

**TABLE 1** The maximum bowing value of GaAs on Si with DFLs and without DFLs. Each sample was grown on 279-μm- and 725-μm-thick Si substrate

<table>
<thead>
<tr>
<th>Si thickness</th>
<th>Sample A</th>
<th>Sample B</th>
<th>Sample C</th>
<th>Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>279 μm</td>
<td>5.6 μm</td>
<td>5.5 μm</td>
<td>5.6 μm</td>
<td>3 μm</td>
</tr>
<tr>
<td>725 μm</td>
<td>36.4 μm</td>
<td>35.4 μm</td>
<td>35.7 μm</td>
<td>32 μm</td>
</tr>
</tbody>
</table>
maximum values of GaAs on Si with thicknesses of 725 μm and 279 μm were 5.6 μm and 36 μm, respectively. The slight increased bowing value of GaAs on Si with DFLs is because of the additional thin DFL layer.

Figure 3 shows the Nomarski imaging and AFM results. Samples A, B, and C comprise InGaP/GaAs, AlGaAs/GaAs, and InGaAs/GaAs DFLs, respectively. The Nomarski images show similar levels of roughness in all samples. To clarify the surface roughness, the root mean square (RMS) values were measured using AFM with a 10-μm² scale, and they show small differences. The RMS values of the control and Samples A, B, and C were 2.224 nm, 1.739 nm, 2.067 nm, and 1.288 nm, respectively. Sample C has the most atomically flat surface among the samples. However, the ECCI images showed significant differences (Figure 4). The TDDs of the control and Samples A, B, and C were 5.3 × 10⁸ cm⁻², 1.7 × 10⁸ cm⁻², 5.1 × 10⁸ cm⁻², and 2.4 × 10⁷ cm⁻², respectively. Sample C showed the minimum TDD value. From the AFM and ECCI results, the strained InGaAs/GaAs DFLs are the most effective to reduce the TDD because the strain relaxation of InGaAs/GaAs DFLs induces the misfit dislocation and the TDD can be reduced by turning the TD into the misfit dislocation [26,27]. The lattice-matched InGaP/GaAs DFLs also show improved flat roughness and lower TDD compared with the control sample. However, the lattice-matched AlGaAs/GaAs DFLs show similar levels of roughness and TDDs to those of the control sample. Because of generating the misfit dislocation from the As/P exchange between the InGaP and GaAs layers, the InGaP/GaAs DFLs are more effective to reduce TDD than AlGaAs/GaAs DFLs [28–30]. Therefore, possibilities to reduce the TDD further using other optimized DFLs, such as compressive strained InGaP/GaAs DFLs, exist. This issue will be explored in a future publication. From our results, the Si substrate thickness, rather than the materials of DFLs, predominantly determines bowing. However, the TDD differs significantly according to the types of DFL materials. Note that the TDD is generated by differences in TEC and the lattice constant and TEC mismatch predominantly causes bowing. As bowing occurred in similar degrees in all DFL samples, TDD, which is reduced by DFLs, cannot be attributed to the TEC mismatch but the lattice constant mismatch. Therefore, the DFLs can block propagate TD, which is caused by the lattice constant mismatch rather than the TEC mismatch. In summary, we found that using thick Si substrates and strained DFLs led to less bowing and minimum TDD; therefore, they are excellent options for GaAs on Si heteroepitaxy for large-scale integration.

4 | CONCLUSION

The monolithic growth of GaAs on Si substrates was studied regarding wafer-scale integration and material characteristics by measuring bowing, analyzing the surface morphology, and conducting ECCI. The bowing of GaAs on Si was investigated by varying the Si substrate thickness, and experimental results were compared with simulation results. Only 3-μm bow was observed when a 725-μm-thick Si substrate was used. The bowing
results show similar levels of bowing in all samples with DFLs, indicating that the Si substrate’s thickness predominantly determines bowing. The surface morphology analysis and ECCI results show that the compressive strained InGaAs/GaAs DFLs show the flattest surface between the DFL samples with an RMS value of 1.288 nm and a minimum TDD value of $2.4 \times 10^4$ cm$^{-2}$. For the lattice-matched DFLs, the InGaP/GaAs DFLs were more effective to reduce the TDD than the AlGaAs/GaAs DFLs by a factor of three. Finally, we found that the TDD reduction by DFLs could be attributed to the lattice constant mismatch, and the strained DFLs on the 725-μm-thick Si substrate can be used for large-scale GaAs integration on Si with less bowing and low TDD.

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