최소 delay를 갖는 buffer 회로의 설계

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A Design of The Buffer Circuit having Minimum Delay Time

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ABSTRACT

The buffer circuit having minimum delay time is designed and analyzed in this paper. Considering the parasitic components of the MOS transistor, the optimal transistor size ratio between the individual buffer stages is presented. This paper's result is better than that of the Mead and Conway's analysis [1] with respect to both delay time and total area that buffer occupies.

I. INTRODUCTION

In VLSI systems, it is always necessary to drive large capacitance loads (e.g. bus lines, clock lines, off-chip circuitry, etc.). In this cases, the ratio of the capacitance that must be driven to the input capacitance, in other words the driving capabilities, of a driving circuit on the chip is often many orders of magnitude, causing a serious signal delay, roughly proportional to the ratio of the size difference, and severe degradation of the overall system performance. To minimize the total delay of this cases, normally the staged buffer is used. The ratio between the individual buffer stages was determined by the classical analysis of Mead and Conway in which the optimal value of the ratio is given by e. However this analysis used too simplified RC delay model, in real world the minimum value of total delay isn't exist at the ratio of e, but at the ratio a little larger than e by 1-2. We describe the reason of this and the procedure of finding the transistor size ratio of the buffer stages having the minimum total delay time considering the parasitic circuit elements of the MOS transistor, particularly the output capacitance.

In section II, the parasitic elements of the CMOS inverter is analyzed. Section III describes the design of optimal buffer circuits and section IV describes the area considerations. This design is verified by circuit simuation using SPICE [2] given at Section IV.

II. PARASITIC ELEMENTS OF CMOS INVERTER

The CMOS inverter has the parasitic circuit elements as shown Fig.1. The output capacitance of CMOS inverter which is comparable to the input capacitance has important impact on the buffer circuit design. Now we analize the component of the output capacitance. The Cin,i is the input capacitance given by

$$C_{in,i} = f(i).C_{in,min} \qquad (1)$$

where, $C_{in,min}$ is the input capacitance of the basic inverter.
$C_{in,min} = C'_{ox}.W_{min}.L_{min}$
$f(i)$ is the ratio of the input capacitance to the basic inverter.

$C_{out,i}$ is the output capacitance considering the drain junction capacitance and the Miller output capacitance of the gate-drain capacitance given by

$$C_{out,i} = K_{eq}.(C_{dbn}+C_{dbp}+C_{jswn}+C_{jswp}) + 2(C_{dgn}+C_{dgp}) \qquad (2)$$

where, K_{eq} is the correcting facter which approximate the voltage dependent capacitance to the eqivalent voltage independent capacitance [3]. This is represented as equation (3).

$$K_{eq} = -\frac{1}{V2-V1}\frac{\phi_o^{m}}{1-m}\left[(\phi_o-V2)^{m}-(\phi_o-V1)^{m}\right] \qquad (3)$$

where, ϕ_o is the built-in junction potential

$$\phi_o = V_t \ln \frac{N_a N_d}{n_i^2}$$

m is the grading coefficient.
m = 1/2 (abrupt junction)
m = 1/3 (graded junction)
V2 is the voltage applied to the junction at the low state of output, viz. -Vol.
V1 is the voltage applied to the junction at the high state of output, viz. -Voh.

To determine the value of $C_{out,i}$, detailed layout information is required as shown Fig.2. With this data, $C_{out,i}$ of NMOS part is given by

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$$C_{out,in} = K_{eq}(C_{dbn}.W_i.L_{dr}+C_{jswn}.2(W_i+L_{dr})) + 2C_{dgn}.W_i = a_n.f(i).C_{in,min}+b_n.f(i).C_{in,min} \quad (4)$$

where,
$a_n = K_{eq}[(C_{dbn}/C'_{ox}).L_{dr}+2C_{jswn}/C'_{ox}].1/L_{min}$
$b_n = 2\ (\ C_{dgn}/C'_{ox}\ )\ 1/L_{min}$

Therefore $C_{out,i}$ is as follows.

$$C_{out,i} = C_{out,i,n}+C_{out,i,p} = (a_n+b_n).f(i).C_{in,min,n} + (a_p+b_p).f(i).C_{in,min,p}$$

Normally $(a_n \approx a_p)=a$, $(b_n \approx b_p)=b$, where a and b are constant at a given process. Therefore $C_{out,i}$ is given by

$$C_{out,i} = (a+b).f(i).C_{in,min} \quad (5)$$

III. DESIGN CONSIDERATIONS

When the gate output drives the large capacitive load which is much larger than the input capacitance of the gate circuit, the total delay increases almost linearly with load capacitance. To minimize the delay of this, the staged buffer as Fig.3 was used.

Assuming N stage, total delay T is given by

$$T = \sum_{i=0}^{N} R_i.C_{i+1} \quad (6)$$

where, $C_{N+1} = C_L$
R_i is the effective resistance of the i'th stage.
$R_i = R_o/f(i)$, where R_o is of minimum inverter.
C_{i+1} is the load capacitance of the i'th stage.
$C_i = (a+b).f(i).C_o+f(i+1).C_o$, where C_o is the input capacitance of the minimum inverter.
$f(0)$ is 1 by definition.

$$\text{Hence, } T = \sum_{i=0}^{N} R_i.C_{i+1} = \sum R_i[(a+b).f(i).C_o+f(i+1).C_o] = R_o.C_o \sum [a+b+f(i+1)/f(i)] = \tau \sum [a+b+f(i+1)/f(i)] = \tau \sum g(i) \quad (7)$$

The requirement to have a minimum value of T satisfying the constraint

$$\prod_{i=0}^{N+1} f(i) = C_L/C_o \quad \text{is}$$

$g(i)$ = constant.
viz., $f(i+1)/f(i) = f$ = constant (8)

Using this result, total delay is given by

$$T = \tau \sum (a+b+f) = (N+1)(a+b+f)\ \tau \quad (9)$$

Since the load capacitance C_L is given by

$$C_L = f^{N+1} C_o.$$

$N+1$ is as follows,

$$N+1 = \ln(C_L/C_o) / \ln(f) \quad (10)$$

Substituting (10) to (9),

$$T = \ln(C_L/C_o)\ (a+b+f)/\ln(f)\ \tau \quad (11)$$

To find out the ratio f at which the total delay T has the minimum value, take the differential with respect to f.

$$dT/df = \ln(C_L/C_o)\ \tau\ [(a+b+f)/\ln(f)]' = 0 \quad (12)$$

Therefore the optimal value of f satisfies

$$\ln(f) = (a+b+f)/f\ . \quad (13)$$

With this value, total delay T is

$$T = \ln(C_L/C_o)\ f\ \tau\ . \quad (14)$$

The plot of total delay T with respect to the size ratio f is given by Fig.4 where the result of Mead and Conway which did'nt consider the effect of the parasitic component, was compared.

IV. AREA CONSIDERATIONS

The total area occupied by the buffer circuits considering the gate area and the interfacing area between the buffer stages is given by

$$A = \sum_{i=0}^{N} [f^i.A_{min}+I(i)]$$

In general, the interfacing area I(i) is almost same, therefore A is

$$A = \frac{1-f^{N+1}}{1-f} A_{min} + (N+1)\ I$$

$$= (1-f^{\ln(C_L/C_o)/\ln(f)})\ A_{min}/(1-f) + \ln(C_L/C_o).I/\ln(f)$$

where, $A_{min} = W_{min,n} L_{min,n} + W_{min,p} L_{min,p}$.

This area is monotonically decreasing function of f, that is the larger f is, the smaller the total area is.

V. SIMULATION RESULT

To justify the result of Section III, SPICE simulation was used with the parameter as shown in Fig.6 and Fig.8. In this cases, the constant K_{eq}, a, and b is given by

$K_{eq} = 0.54$
$a = 1.7$
$b = 0.7$

Therefore (13) shows the optimal ratio as

$$f = 4.6$$

With this value, the result of Mead & Conway was compared in the cases with considering the output capacitance or without, respectively. First, considering the output junction capacitance, the result is as shown by Fig.5 with the SPICE input file given by Fig.6. As we know from Fig.5, the ratio determined by this paper's result is better, although the

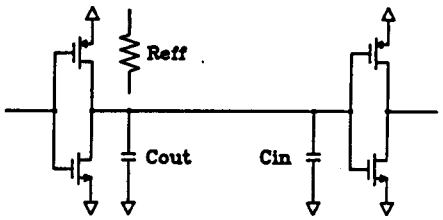
difference is minor. Second, without considering the output capacitance, that is in SPICE input file the AD, AS, PS, and PD is given as 0, the simulation result shows that the difference between f=4.6 and e is almost zero as Fig.7 and Fig.8. These simulation results certifies the theory of this paper very well.

VI. CONCLUSION

The design of buffer circuit having minimum delay was described considering the output capacitance of the inverter. The result is that when ln(f)=(a+b+f)/f, the speed and area respect is much better than the classical Mead and Conway result, i.e. f=e.

REFERENCES

[1] C. Mead and L. Conway, " Introduction to VLSI system, " pp.12-14, Addison Wesley, Reading Mass, 1980
[2] L.W. Nagel, " SPICE2: A Computer Program to Simulate Semiconductor Circuits, " Memo ERL-M520, University of California, Berkeley, CA, May 9, 1975
[3] D.A. Hodges and H.G. Jackson, " Analysis and design of digital integrated circuits, " , p.137, McGraw-Hill, New York, 1983



delay = Reff • (Cin+Cout)

Fig.1 The parasitic circuits elements of the CMOS inverter.

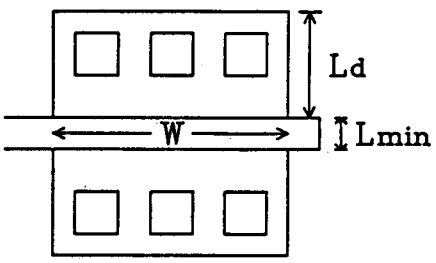


Fig.2 The NMOS part layout of the inverter

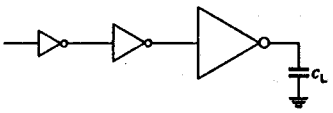


Fig.3 The staged buffer

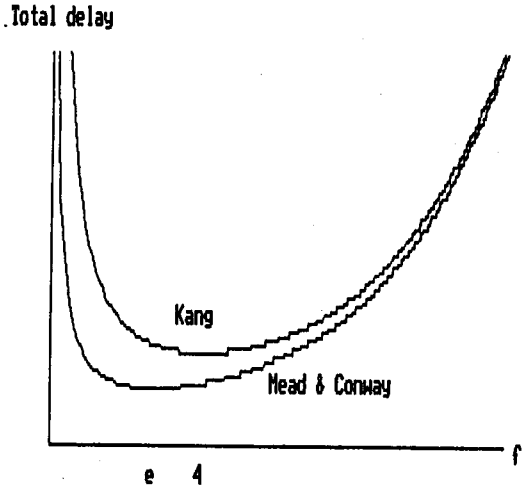


Fig.4 Total delay vs Size ratio

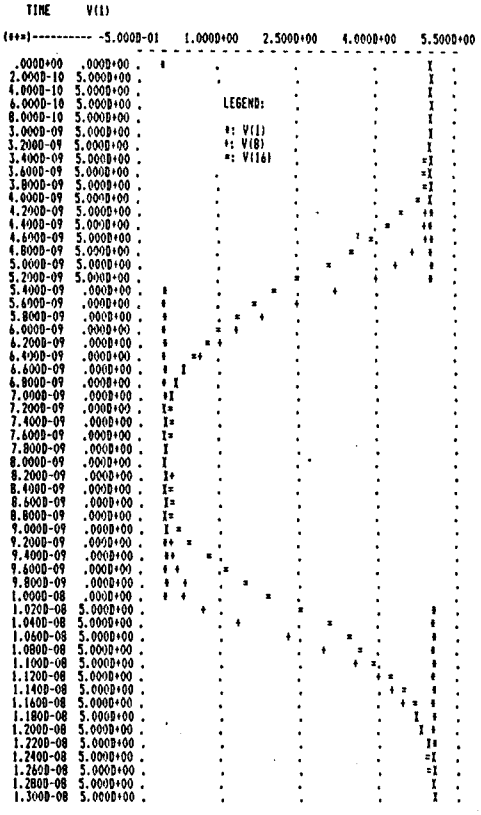


Fig.5 Simulation result

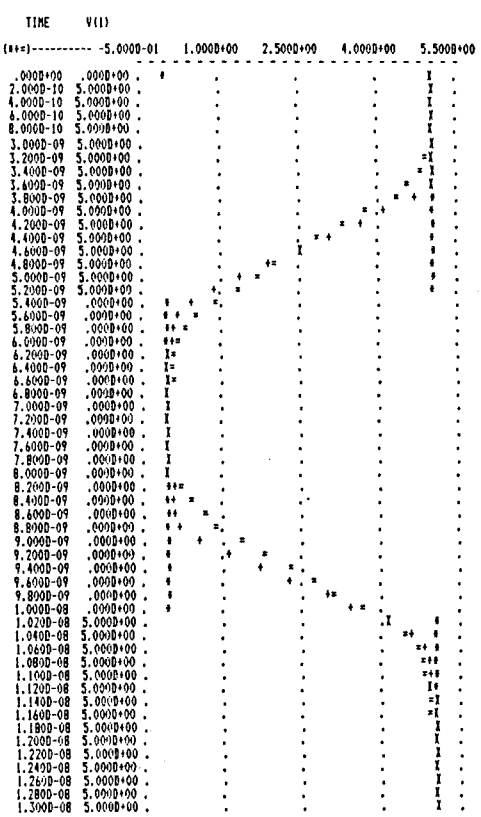


Fig.7 Simulation result when the parasitic components is ignored.

```
VDD 100 0 5
VIN  1 0 PULSE(0 5 0N 0N 0N 5N 10N)
MP1  2  1  100 100 MP  W=8U      L=3U AD=80P    AS=80P    PD=28U     PS=28U
MN1  2  1    0   0 MN  W=4U      L=3U AD=40P    AS=40P    PD=24U     PS=24U
MP2  3  2  100 100 MP  W=21.6U   L=3U AD=216P   AS=216P   PD=41.6U   PS=41.
MN2  3  2    0   0 MN  W=10.8U   L=3U AD=108P   AS=108P   PD=30.8U   PS=30.
MP3  4  3  100 100 MP  W=59.2U   L=3U AD=592P   AS=592P   PD=79.2U   PS=79.
MN3  4  3    0   0 MN  W=29.6U   L=3U AD=296P   AS=296P   PD=49.6U   PS=49.
MP4  5  4  100 100 MP  W=160.8U  L=3U AD=1608P  AS=1608P  PD=180.8U  PS=180.
MN4  5  4    0   0 MN  W=80.3U   L=3U AD=803P   AS=80.3P  PD=100.3U  PS=100.
MP5  6  5  100 100 MP  W=436.8U  L=3U AD=4368P  AS=4368P  PD=456.3U  PS=456.
MN5  6  5    0   0 MN  W=218.4U  L=3U AD=2184P  AS=2184P  PD=238.4U  PS=238.
MP6  7  6  100 100 MP  W=1187.2U L=3U AD=11872P AS=11872P PD=1207.2U PS=120
MN6  7  6    0   0 MN  W=593.6U  L=3U AD=5936P  AS=5936P  PD=613.6U  PS=613.
MP7  8  7  100 100 MP  W=3228U   L=3U AD=32280P AS=32280P PD=3248U   PS=324
MN7  8  7    0   0 MN  W=1614U   L=3U AD=16140P AS=16140P PD=1814U   PS=181
MP8  9  8  100 100 MP  W=8192U   L=3U AD=81920P AS=81920P PD=8212U   PS=821
MN8  9  8    0   0 MN  W=4386U   L=3U AD=43860P AS=43860P PD=4406U   PS=440

VIN2 11 0 PULSE(0 5 0N 0N 0N 5N 10N)
MP11 12 11 100 100 MP  W=8U     L=3U AD=80P    AS=80P    PD=28U     PS=28U
MN11 12 11   0   0 MN  W=4U     L=3U AD=40P    AS=40P    PD=24U     PS=24U
MP12 13 12 100 100 MP  W=32U    L=3U AD=320P   AS=320P   PD=52U     PS=52U
MN12 13 12   0   0 MN  W=16U    L=3U AD=160P   AS=160P   PD=36U     PS=36U
MP13 14 13 100 100 MP  W=128U   L=3U AD=1280P  AS=1280P  PD=148U    PS=148U
MN13 14 13   0   0 MN  W=64U    L=3U AD=640P   AS=640P   PD=84U     PS=84U
MP14 15 14 100 100 MP  W=512U   L=3U AD=5120P  AS=5120P  PD=532U    PS=532U
MN14 15 14   0   0 MN  W=256U   L=3U AD=2560P  AS=2560P  PD=276U    PS=276U
MP15 16 15 100 100 MP  W=2048U  L=3U AD=20480P AS=20480P PD=2068U  PS=2068U
MN15 16 15   0   0 MN  W=1024U  L=3U AD=10240P AS=10240P PD=1044U  PS=1044U
MP16 17 16 100 100 MP  W=8192U  L=3U AD=81920P AS=81920P PD=8212U  PS=8212U
MN16 17 16   0   0 MN  W=4386U  L=3U AD=43860P AS=43860P PD=4406U  PS=4406U

.OP
.TRAN 0.2N 50N
.OPTIONS LIMPTS=500
.PRINT TRAN V(1) V(8) V(15)
.PLOT  TRAN V(1) V(8) V(16) (-0.5 5.5)

***** CMOS SPICE PARAMETER ( 4um p-well ) *****
.MODEL MP PMOS LEVEL=2
+ VTO=-0.74  KP=34.3E-6  NSUB=7.1E14  GAMMA=0.63   LD=0.5U       TOX=0.05U
+ XJ=1.14U   LAMBDA=0.02 UO=231.5     UCRIT=0.54E5 UEXP=0.28     PHI=0.78
+ VMAX=0.58E5  NEFF=5      MJ=0.46      CJ=1.43E-4  CJSW=2.45E-10 MJSW=0.72
+ CGSO=4.0E-10 CGDO=4.0E-10 CGBO=1.4E-10 NFS=1.49E11
* delta W = 1.78um , delta L = -0.66um
.MODEL MN NMOS LEVEL=2
+ VTO= 0.71  KP=0.40E-4  NSUB=1.57E16 GAMMA=0.59   LD=0.65U      TOX=0.05U
+ XJ=0.89U   LAMBDA=0.02 UO=603.93    UCRIT=0.70E5 UEXP=0.11     PHI=0.64
+ VMAX=0.61E5 NEFF=5      MJ=0.514     CJ=3.695E-4 CJSW=4.174E-10 MJSW=0.441
+ CGSO=4.0E-10 CGDO=4.0E-10 CGBO=1.4E-10 NFS=2.28E11
* delta W = 1.68um , delta L = -0.19um
.END
```

Fig.6 Input file of Fig.5

```
VDD 100 0 5
VIN  1 0 PULSE(0 5 0N 0N 0N 5N 10N)
MP1  2  1  100 100 MP  W=8U  L=3U
MN1  2  1    0   0 MN  W=4U  L=3U
MP2  3  2  100 100 MP  W=21.6U L=3U
MN2  3  2    0   0 MN  W=10.8U L=3U
MP3  4  3  100 100 MP  W=59.2U L=3U
MN3  4  3    0   0 MN  W=29.6U L=3U
MP4  5  4  100 100 MP  W=160.8U L=3U
MN4  5  4    0   0 MN  W=80.3U  L=3U
MP5  6  5  100 100 MP  W=436.8U L=3U
MN5  6  5    0   0 MN  W=218.4U L=3U
MP6  7  6  100 100 MP  W=1187.2U L=3U
MN6  7  6    0   0 MN  W=593.6U  L=3U
MP7  8  7  100 100 MP  W=3228U L=3U
MN7  8  7    0   0 MN  W=1614U L=3U
MP8  9  8  100 100 MP  W=8192U L=3U
MN8  9  8    0   0 MN  W=4096U L=3U

VIN2 11 0 PULSE(0 5 0N 0N 0N 5N 10N)
MP11 12 11 100 100 MP  W=8U L=3U
MN11 12 11   0   0 MN  W=4U L=3U
MP12 13 12 100 100 MP  W=32U L=3U
MN12 13 12   0   0 MN  W=16U L=3U
MP13 14 13 100 100 MP  W=128U L=3U
MN13 14 13   0   0 MN  W=64U  L=3U
MP14 15 14 100 100 MP  W=512U L=3U
MN14 15 14   0   0 MN  W=256U L=3U
MP15 16 15 100 100 MP  W=2048U L=3U
MN15 16 15   0   0 MN  W=1024U L=3U
MP16 17 16 100 100 MP  W=8192U L=3U
MN16 17 16   0   0 MN  W=4386U L=3U

.OP
.TRAN 0.2N 50N
.OPTIONS LIMPTS=500
.PRINT TRAN V(1) V(8) V(15)
.PLOT  TRAN V(1) V(8) V(16) (-0.5 5.5)

***** CMOS SPICE PARAMETER ( 4um p-well ) *****
.MODEL MP PMOS LEVEL=2
+ VTO=-0.74  KP=34.3E-6  NSUB=7.1E14  GAMMA=0.63   LD=0.5U       TOX=0.05U
+ XJ=1.14U   LAMBDA=0.02 UO=231.5     UCRIT=0.54E5 UEXP=0.28     PHI=0.78
+ VMAX=0.58E5  NEFF=5      MJ=0.46      CJ=1.43E-4  CJSW=2.45E-10 MJSW=0.72
+ CGSO=4.0E-10 CGDO=4.0E-10 CGBO=1.4E-10 NFS=1.49E11
* delta W = 1.78um , delta L = -0.66um
.MODEL MN NMOS LEVEL=2
+ VTO= 0.71  KP=0.40E-4  NSUB=1.57E16 GAMMA=0.59   LD=0.65U      TOX=0.05U
+ XJ=0.89U   LAMBDA=0.02 UO=603.93    UCRIT=0.70E5 UEXP=0.11     PHI=0.64
+ VMAX=0.61E5 NEFF=5      MJ=0.514     CJ=3.695E-4 CJSW=4.174E-10 MJSW=0.441
+ CGSO=4.0E-10 CGDO=4.0E-10 CGBO=1.4E-10 NFS=2.28E11
* delta W = 1.68um , delta L = -0.19um
.END
```

Fig.8 Input file of Fig.7