A 32x33 Photo-elements MOS Image Sensor

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Abstract

A 32x33 MOS-type area image sensor has been fabricated. The blooming current is reduced to 1/14 by forming +p photocell in P-well instead of a simple p-type substrate. A shallow n+ junction is made to improve the sensitivity of photodiode on short wavelength. Bootstrapping circuit technique is applied to obtain high speed dynamic shift register. The shift register operates at up to 10MHz for 7V clock.

I. Introduction

Solid-state image sensor has the advantages of small size, light weight, low power dissipation and mass production possibility compared to image pick-up tube. However, it is difficult to improve resolution in solid-state image sensor because there is a limitation in dynamic range due to smear noise and fixed pattern noise(FPN). Blooming phenomenon is also serious problem to be controlled. It is necessary to make a high speed shift register to gain high speed scan rate as the number of pixels increases. In this paper, P-well is formed in N-type substrate to suppress blooming and smear noise, and shallow junction photodiode is used to make good spectral response, especially to blue color and to suppress FPN noise. Bootstrapcircuit is used to achieve the high speed scan of a shift register.

This paper reports a MOS type 32x33 area image sensor which is processed by adopting a conventional MOS technology. In section II and III, the design and the measured results of the image sensor are described, respectively.

II. Design

Fig. 1 shows the whole features of image sensor. A photosignal generated in a $n^{+}p$ photodiode can be read out by MOS switches. Fig. 2 shows the equivalent circuit for the image cell, MOS switches and output elements. Refering to the timing diagram of driving clock shown in Fig. 3, when VMOS becomes ON by Ov, the charge accumulated in the photodiode is transferred to C_V. When the horizontal clock $Ø_H$ becomes high, the charge is transferred from C_V to C_H and to the

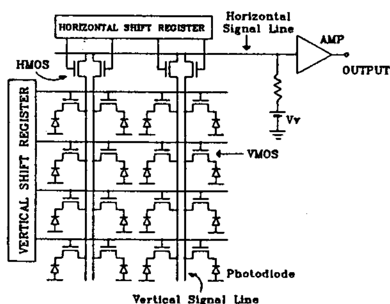


Fig. 1 Schematic diagram of (a) area image sensor

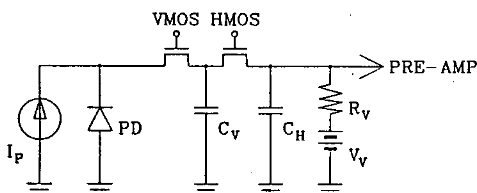


Fig. 2 Equivalent circuit for signal read out

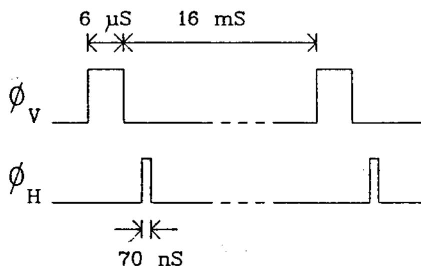


Fig. 3 Driving clock of the circuit of Fig. 2

output stage. To achieve maximum transfer of signal charges, the condition $C_{PD} << C_V << C_H$ must be satisfied. The parasitic capacitors mainly formed by metal line are utilized for C_V and C_H.

1. Photocell

A pixel is composed of a photodiode and a VMOS shown in Fig. 4. The sensitivity depends upon wavelength and n+ junction depth, that is, as the junction becomes deeper, the sensitivity for short wave decreases. Thus a shallow

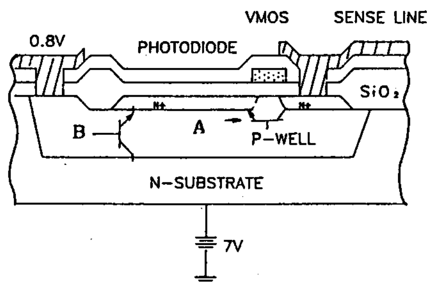


Fig. 4 Schematic cross-sectional view of a unit cell

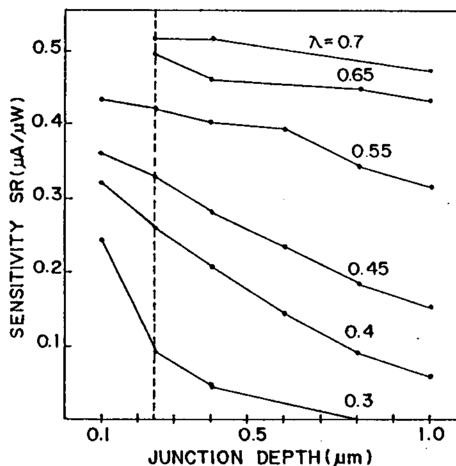


Fig. 5 Simulation results of a photodiode depending on wavelength(λ) and n+ junction depth

junction process is adopted to increase the blue sensitivity. The simulation results are shown in Fig. 5, where the junction depth represented by the dotted vertical line is the value of process target.

2. Low noise P-well structure.

It is important to prevent smear noise and blooming inevitably occurring in sensing part of the image sensor. The two noises can be reduced by using P-well structure. The carriers which are generated in deep P-type region can not diffuse into other pixels by forming

P-well structure because of the reverse bias between the substrate and P-well. When the incident light is very strong, the photodiode becomes saturated, and the bias of n^+p diode converts into forward from reverse enough to turn on the horizontal bipolar transistor shown in Fig. 4(B). As a result, the accumulated charge in photodiode transferred to C_V to make blooming. To suppress blooming, the vertical overflow drain structure shown in Fig. 4(A) is formed.

3. High speed dynamic shift register

The circuit shown in Fig. 6 is used for a unit stage of the high scan rate shift register. Here, C_B is a bootstrap capacitor which is a kind of gate capacitor. Since C_B is much larger than usual parasitic capacitances, V_S becomes as high as V_D when it is high level. By obtaining $V_S = V_D$, V_D level is sustained at each stage and high scan speed can be achieved. In this figure, V_S represents the low level of the driving clock.

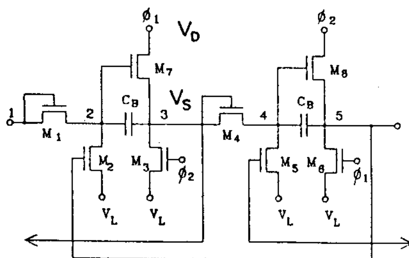


Fig. 6 Unit stage circuit of horizontal shift register

4. System

Fig. 7 shows photograph of a 32x33 area image sensor. A, B and C in the figure stand for a horizontal shift register, a vertical shift register and a cell array, respectively.

III. Results

The spectral response of the photodiode is shown in Fig. 8. The circuit shown in Fig. 9 was constructed to measure the discharge characteristics of the photodiode. The discharge characteristics are shown in Fig. 10, which shows the saturation voltage of 0.5V. The blooming currents depending on the low voltage of VMOS, the substrate voltage, and the drain voltage(video bias) measured using circuit demonstrated in Fig. 4 are shown in Fig. 11 (a), (b), (c). The minimum operation high voltage of the horizontal shift register is measured and shown in Fig. 12. The sensor system shown in Fig. 7 promises the possibility to construct a large system which can give high resolution, wide dynamic

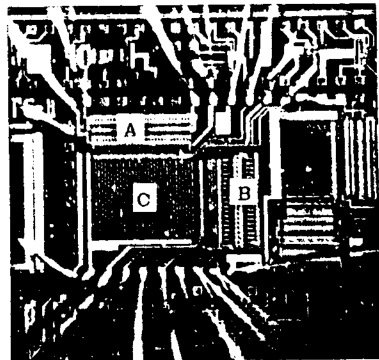


Fig. 7 Photograph of 32x33 area image sensor

range, and relatively low smear and blooming noise.

IV. Conclusion

An image sensor composed of 32x33 photoelements and vertical and horizontal

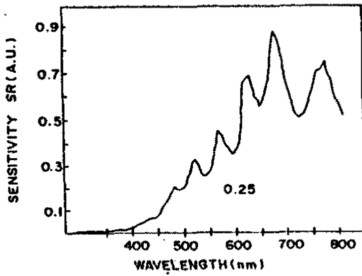


Fig. 8 Spectral response of n+p photodiode with junction depth 0.25um

shift registers has been realized. n^+pn structure of the photocell shows the maximum response at 650nm. It is compared to 800nm for n^+p diode. The blooming current was reduced to 1/14 of n^+p cell. This improvement is also due to n^+pn structure. It was successful to operate the system at 7.16MHz with saturation incident light of 260lux.

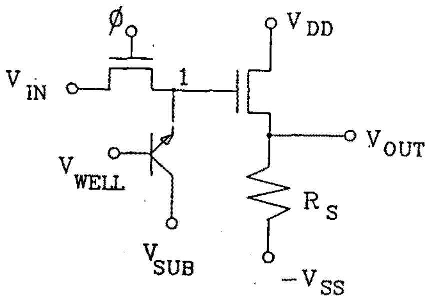


Fig. 9 Measurement circuit of the discharge characteristics of photodiode

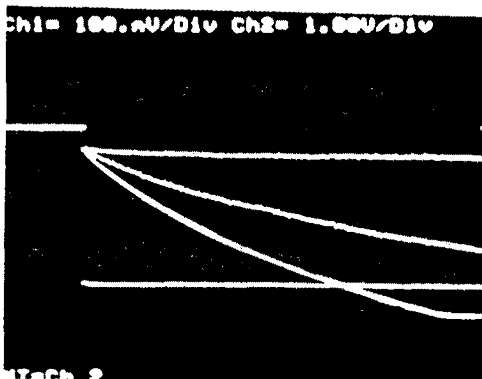
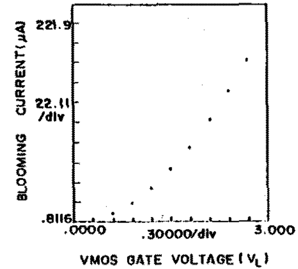
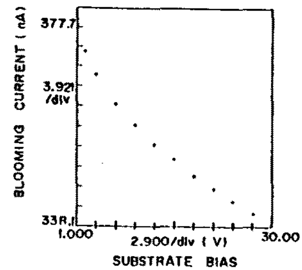


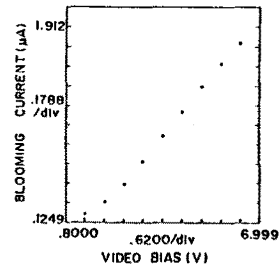
Fig. 10 Discharge characteristics of photodiode



(a)



(b)



(c)

Fig. 11 Blooming current depending on VMOS gate voltage(a), substrate bias(b) and video bias(c)

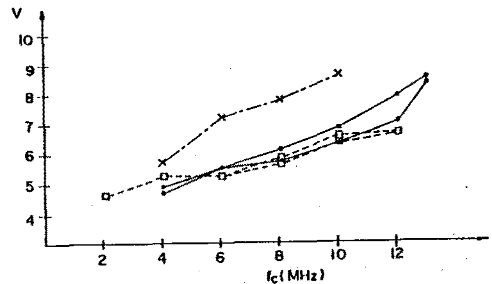


Fig. 12 Minimum operation voltage of clock depending on operation frequency

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