A Self-Consistent Analytic Threshold Voltage Model for Thin SOI N-channel MOSFET

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ABSTRACT

An accurate analytical threshold model is presented for fully depleted SOI which has a Metal-Insulator-Semiconductor-Insulator-Metal structure. The threshold voltage is defined as the gate voltage at which the second derivative of the inversion charge with respect to the gate voltage is maximum. Therefore the model is self-consistent with the measurement scheme. Numerical simulations show good agreement with the model with less than 3% error.

NOTATION

V_{gf} : front gate voltage
V_{gb} : back gate voltage
V_{ffb} : front gate flat band voltage
V_{bfb} : back gate flat band voltage
ϕ_{fs} : surface potential in the Si film at the front interface
ϕ_{bs} : surface potential in the Si film at the back interface
E_{fs} : electric field in the Si film at the front interface
E_{bs} : electric field in the Si film at the back interface
Q_{Si} : total depletion charge in Si film ($=qN_a t_{Si}$)
Q_n : total inversion charge in the Si film
t_{Si} : thickness of the Si film
t_{fox}, t_{box} : thicknesses of the front and back oxides
ϵ_s : permittivity of Si
ϵ_{ox} : permittivity of oxide
V_t : thermal voltage
T : absolute temperature
N_a : acceptor doping concentration of Si film
ϕ_p : absolute value of the bulk Fermi potential
C_{Si} : depletion capacitance of the silicon film($=\epsilon_s/t_{Si}$)
C_{fox} : front gate oxide capacitance($=\epsilon_{ox}/t_{fox}$)
C_{box} : back gate oxide capacitance($=\epsilon_{ox}/t_{box}$)
Q_{ff} : front oxide to silicon interface charge density
Q_{bf}: back oxide to silicon interface charge density

I. INTRODUCTION

MOSFET's made on Silicon-On-Insulator(SOI) structures provide several attractive features, such as latch-up free operation, high speed, high integration density, radiation hardness[1,2]. During the last few years, several authors have reported that the kink effect[3] in thick SOI structures can be eliminated by reducing the film thickness and improved device characteristics such as higher subthreshold slope[4], higher carrier mobility[5], and the reduction of short channel effect[6] can be obtained in fully depleted SOI MOSFET's. Due to these attractive features and the availability of high quality SOI wafers prepared by either SIMOX or ZMR, fully depleted SOI MOSFET's are expected to be used widely in future VLSI's, and thus, an accurate modeling of these MOSFET's which is consistent with the measurement scheme is becoming a fundamental problem.

Most of the previous works related to the threshold voltage modeling of SOI MOSFET are based on the traditional definition of the threshold voltage which says that at the onset of strong inversion, the band bending in silicon is twice the bulk Fermi potential[7-9]. This definition, however, becomes questionable[10] for fully depleted SOI MOSFET's since it is well known that there is significant bulk conduction in these devices. Also, this definition of threshold voltage may not be consistent with the measurement method which is based on the I-V characteristics rather than the band bending inside silicon. Thus, there is a need for a mathematically well-defined threshold voltage which is self consistent with the measurement method and can be applied for wide variations of the parameters such as the film thickness, doping concentration, oxide thickness, and interface charges both at the front and back silicon interfaces.

We report in this paper an analytical threshold voltage model of a long channel SOI MOSFET. The threshold voltage is defined as the gate voltage at which the second derivative of the inversion charge or drain current for small drain voltages with respect to the gate voltage is maximum[11]. For the sake of simplicity of calculation, uniform channel doping is assumed. The results of the threshold voltage based on the model are then compared with two-dimensional device simulation results.

II. MODEL FORMULATION

General n-channel SOI MOSFET structure and energy band diagram are shown in Fig.1. Fig.2 shows the inversion charge density simulated at a threshold voltage as a function of SOI film thickness. The inversion charge density is distributed to broaden as the SOI film thickness is decreased. The fraction of surface charge also decreases with decreasing SOI film thickness. Threfore it is difficult to find accurate threshold voltage without considering inversion charge density. To solve accurate threshold voltage, we assume that the inversion charge is distributed with an exponential function along the distance x at the front surface of the silicon film when the drain bias is small. Then the inversion charge density n(x) at a distance x can be expressed as

$$n(x) = n_o \exp(-x / \lambda). \quad (1)$$

Using the relationship

$$N_a = n_i \exp(\phi_p / V_t),$$

n_o can be written as

$$n_o = N_a \exp[(\phi_{fs} - \phi_p) / V_t].$$

The characteristic length, λ, is related to the electric field at the front surface, E_{fs}, by

$$\lambda = \frac{V_t}{E_{fs}} = \frac{C_{Si} V_t}{\epsilon_s E_{fs}} t_{Si}.$$

Then, Q_n becomes

$$Q_n = \int_0^{t_{Si}} q n_o \exp(-x / \lambda)\, dx. \qquad (2)$$

For $\lambda << t_{Si}$, Eq.(2) is simplified to

$$Q_n = Q_{Si} \frac{\lambda}{t_{Si}} \exp[(\phi_{fs} - \phi_p) / V_t]$$

$$= Q_{Si} \frac{C_{Si} V_t}{\epsilon_s E_{fs}} \exp[(\phi_{fs} - \phi_p) / V_t]. \qquad (3)$$

With the assumption of exponential distribution for electrons, the Poisson's equation

$$\frac{d^2\phi(x)}{dx^2} = -\frac{q}{\epsilon_s}[-n(x) - N_a], \qquad (4)$$

can be integrated once with the boundary condition $E(x=0) = E_{fs}$ to obtain

$$\frac{d\phi}{dx} = \frac{qN_a}{\epsilon_s} x + \frac{1}{\epsilon_s} \int qn(x)dx - E_{fs}$$

$$= \frac{Q_{Si}}{\epsilon_s} \frac{x}{t_{Si}} + \frac{Q_n(x)}{\epsilon_s} - E_{fs}. \qquad (5)$$

For $x = t_{Si}$, Eq.(5) becomes

$$\epsilon_s E_{fs} = \epsilon_s E_{bs} + Q_{Si} + Q_n. \qquad (6)$$

Integrating Eq.(5) once again with the boundary condition, $\phi(x=0) = \phi_{fs}$,

$$\phi(x) = \phi_{fs} + \frac{Q_{Si}}{2\epsilon_s} \frac{x^2}{t_{Si}} + - E_{fs} x + \frac{1}{\epsilon_s} \int_0^{x} Q_n(x)dx. \qquad (7)$$

For $x = t_{Si}$, Eq.(7) becomes

$$\phi_{bs} = \phi_{fs} + \frac{Q_{Si}}{2C_{Si}} - \frac{\epsilon_s E_{fs}}{C_{Si}} + \frac{1}{\epsilon_s} \int_0^{t_{Si}} Q_n(x)dx. \qquad (8)$$

Noting that $\lambda << t_{Si}$, the last term in Eq.(8) can be approximated as

$$\frac{1}{\epsilon_s} \int_0^{t_{Si}} Q_n(x)dx = \frac{Q_n}{\epsilon_s} t_{Si} \left(1 - \frac{\lambda}{t_{Si}}\right)$$

$$= \frac{Q_n}{\epsilon_s} t_{Si} = \frac{Q_n}{C_{Si}}. \qquad (9)$$

Thus

$$\phi_{bs} = \phi_{fs} + \frac{Q_{Si}}{2C_{Si}} - \frac{\epsilon_s E_{fs}}{C_{Si}} + \frac{Q_n}{C_{Si}}. \qquad (10)$$

On the other hand, the voltages at the front and back gates are related to the surface potential, gate oxide voltage drop, and bulk Fermi potential, by

$$V_{gf} - V_{ffb} = \phi_{fs} + \frac{\epsilon_s E_{fs}}{C_{fox}} + \phi_p, \qquad (11)$$

$$V_{gb} - V_{bfb} = \phi_{bs} - \frac{\epsilon_s E_{bs}}{C_{box}} + \phi_p. \qquad (12)$$

Substituting Eq.(6) and (10) into Eq.(12) gives

$$\epsilon_s E_{fs} = \alpha C_{Si} (\phi_{fs} + \phi_p) + \alpha C_{Si}(V_{bfb} - V_{gb})$$

$$+ \beta Q_{Si} + Q_n, \qquad (13)$$

where

$$\alpha = \frac{C_{box}}{C_{Si} + C_{box}},$$

$$\beta = \frac{1 + C_{box} / 2C_{Si}}{1 + C_{box}/C_{Si}}.$$

We now have two equations i.e., Eq.(3) and (13), which gives Q_n in terms of ϕ_{fs} and E_{fs}. Combining these two equations, one obtains

$$\frac{Q_n}{Q_{Si}} \left[\epsilon_s \frac{E_{fs}^o}{C_{Si} V_t} + \alpha \frac{\phi_{fs} + \phi_p}{V_t} + \frac{Q_{Si}}{C_{Si} V_t} \frac{Q_n}{Q_{Si}}\right]$$

$$= \exp[(\phi_{fs} - \phi_p)/V_t], \qquad (14)$$

where

$$\epsilon_s E_{fs}^o = \alpha C_{Si}(V_{bfb} - V_{bg}) + \beta Q_{Si}.$$

It is to be noted that the second and third terms inside the bracket on the left hand side of Eq.(14) are negligible compared to the magnitude of the first term. Thus, Eq.(14) can be approximated as

$$\phi_{fs} = \phi_p + V_t \ln \left[\frac{Q_n}{Q_{Si}} \frac{\epsilon_s E_{fs}^o}{C_{Si} V_t}\right]. \qquad (15)$$

The surface potential is a function of doping, inversion charges, front and back gate capacitances, and film thickness.

Substituting Eqs.(15) and (13) into Eq.(11), one obtains

$$V_{gf} = V_{ffb}^{*} + \left(1 + \alpha \frac{C_{Si}}{C_{fox}}\right)\left[2\phi_p + V_t \ln \frac{Q_n}{Q_{Si}} \frac{\epsilon_s E_{fs}^o}{C_{Si} V_t}\right]$$

$$+ \frac{Q_n}{C_{fox}}, \qquad (16)$$

where

$$V_{ffb}^{*} = V_{ffb} + \alpha(V_{bfb} - V_{gb}) \frac{C_{Si}}{C_{fox}} + \beta \frac{Q_{Si}}{C_{fox}}.$$

We note that Eq.(16) is of the form[12]

$$V_{gf} - V_o = A_1 Q_n + A_2 \ln(\frac{Q_n}{Q_o}) \quad (17)$$

and is valid both for subthreshold region and for strong inversion region. Let us define the threshold voltage as the gate voltage where the variation of the transconductance with the gate voltage for small drain bias is maximum. This threshold voltage can easily be measured from the I-V terminal characteristics without regard to the band bending inside the silicon film. If we neglect the variation of mobility with the gate voltage, the threshold voltage is the gate voltage where the second derivation of Q_n with respect to V_{gf} is maximum. As shown in the Appendix, this occurs when

$$Q_n = Q_{no} = \frac{A_2}{2A_1} = \frac{V_t}{2} C_{fox}(1 + \alpha\frac{C_{Si}}{C_{fox}})$$

for Eq.(17). Thus, the threshold voltage is

$$V_{TH} = V^{\bullet}_{ffb} + (1 + \alpha\frac{C_{Si}}{C_{fox}}) [2\phi_p + V_t \ln(\frac{Q_{no}}{Q_{Si}} \frac{\epsilon_s E^o_{fs}}{C_{Si}V_t})]$$

$$+ \frac{Q_{no}}{C_{fox}}.$$

Substituting $V^{\bullet}_{ffb}$, E^o_{fs} and Q_{no},

$$V_{TH} = V_{ffb} + \alpha(V_{bfb} - V_{gb})\frac{C_{Si}}{C_{fox}} + \beta\frac{Q_{Si}}{C_{fox}} + (1 + \alpha\frac{C_{Si}}{C_{fox}})$$

$$(2\phi_p + \frac{V_t}{2} + V_t \ln[\frac{1}{2} (\frac{C_{fox}}{C_{Si}} + \alpha) (\beta + \alpha\frac{V_{bfb} - V_{bg}}{Q_{Si}/C_{Si}})])$$

III. MODEL VERIFICATION AND SIMULATION

Our analytical model has been demonstrated by the two-dimensional simulation. Fig. 3 - 7 show the threshold voltage characteristics according to various conditions. In Fig. 3, our analytical and numerically simulated threshold voltages are plotted as a function of SOI film thickness. As shown in Fig. 3, the analytical model agrees very well with the simulated results even for very thin film case that the inversion charge is broadly distributed over the entire region of the film. As the film thickness increases, the fully depletion condition is not satisfied, dashed line in Fig.3, and then our model is no longer applicable. In addition, the threshold voltage agrees with the simulation results in the wide variation of front gate oxide thickness, as shown in Fig.4. Fig.5 also shows the dependence of the threshold voltage on film doping concentration. Fig. 6 and 7 show the dependence of the threshold voltage on the front and back gate interface charges, respectively. The effect of back gate interface charge density is nearly equal to front gate interface charge density in threshold voltage as shown in Fig.6 and Fig.7.

IV. CONCLUSION

The analytical model is verified to agree well with the 2D numerical simulation results. The model is derived based on the inversion charge concept, thereby being self consistent with the mesurement scheme. In fact, the surface potential at the threshold condition for the thin SOI MOSFET is slightly lower than the bulk Fermi potential. But this effect is usually not considered in the traditional method. Our approach includes the lowering effect of the surface potential and thus, the model can be accurately applicable even to the very thin film case.

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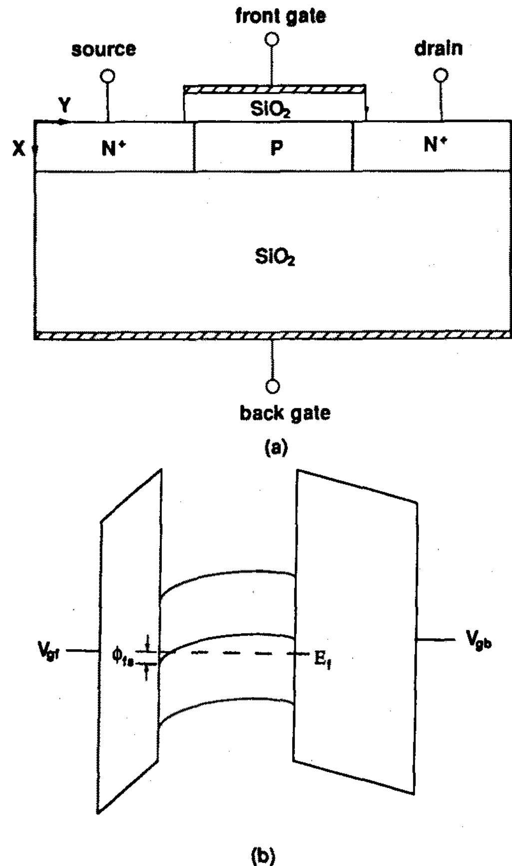

Fig.1 - (a) Cross-section of an n-channel SOI MOSFET.
(b) Energy band diagram when the silicon film is thick. surface potential ϕ_{fs} and the voltage reference are defined.

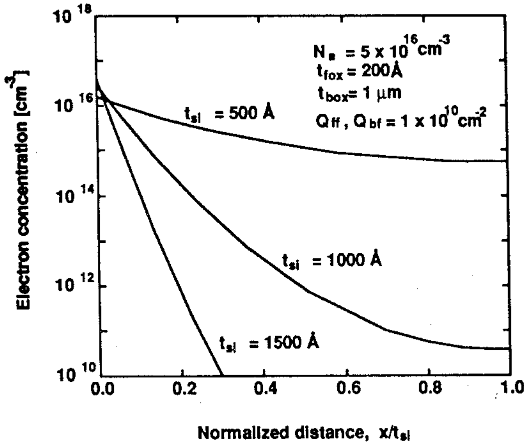

Fig.2 - SOI film thickness dependence of inversion charge distribution at the threshold voltage.

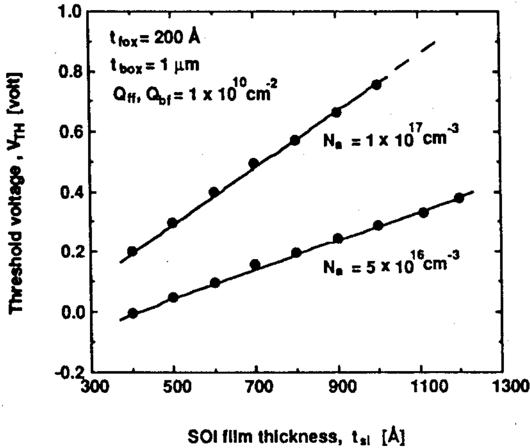

Fig.3 - SOI film thickness dependence of threshold voltage. (----- analytic, ● ● ● simulation)

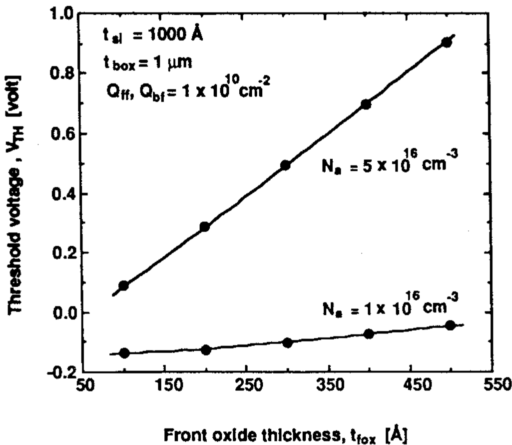

Fig.4 - Front gate oxide thickness dependence of threshold voltage. (----- analytic, ● ● ● simulation)

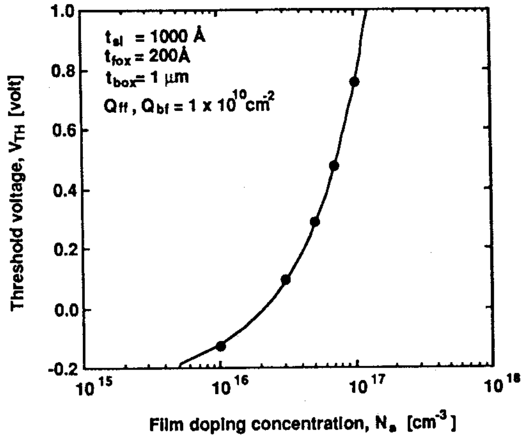

Fig.5 - Film doping concetration dependence of threshold voltage. (----- analytic, ● ● ● simulation)

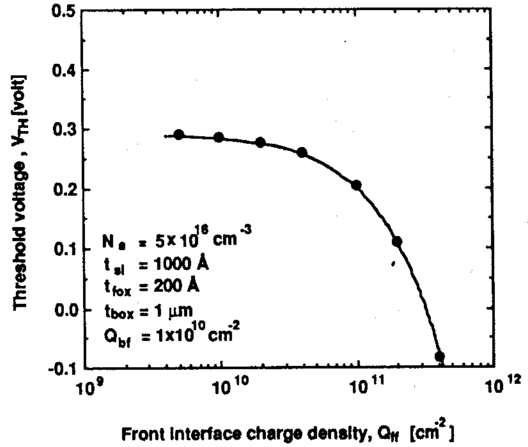

Fig.6 - Front interface charge dependence of threshold voltage. (----- analytic, ● ● ● simulation)

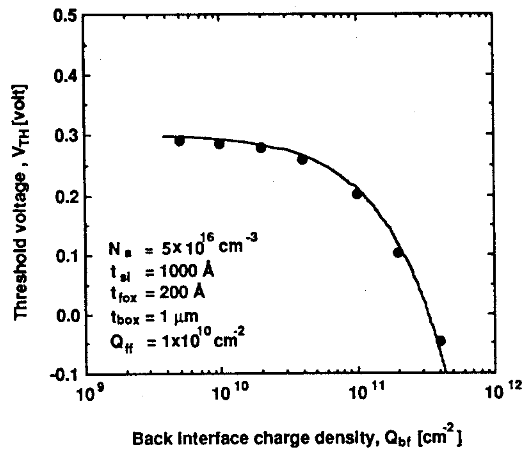

Fig.7 - Back interface charge dependence of threshold voltage. (----- analytic, ● ● ● simulation)

Appendix

The total inversion charge is calculated when d^2Q_n/dV_{gf}^2 is maximum as follows:

$$V_{gf} - V_o = A_1Q_n + A_2 \ln(Q_n/Q_o)$$

$$\frac{dV_{gf}}{dQ_n} = A_1 + \frac{A_2}{Q_n}$$

$$\frac{dQ_n}{dV_{gf}} = \frac{Q_n}{A_2 + A_1Q_n}$$

$$\frac{d^2Q_n}{dV_{gf}^2} = \frac{A_2 + A_1Q_n - A_1Q_n}{(A_2 + A_1Q_n)^2} \frac{Q_n}{A_2 + A_1Q_n}$$

$$= \frac{A_2Q_n}{(A_2 + A_1Q_n)^3}$$

$$\frac{d^3Q_n}{dV_{gf}^3} = \frac{A_2(A_2 + A_1Q_n)^3 - 3(A_2 + A_1Q_n)^2 A_1A_2Q_n}{(A_2 + A_1Q_n)^6}$$

$$\frac{Q_n}{(A_2 + A_1Q_n)}$$

For $d^3Q_n/dV_{gf}^3 = 0$, d^2Q_n/dV_{gf}^2 is maximum.

$$A_2(A_2 + A_1Q_n) - 3A_1A_2Q_n = 0$$

$$A_2^2 - 2A_1A_2Q_n = 0$$

$$Q_n = Q_{no} = \frac{A_2}{2A_1}$$