Fault Diagnosis of Logical Circuit by use of Corrrelation and Neural Network

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Abstract: This paper describes a new method of pseudo-random testing of a digital circuit by use of correlation method and a neural network. The authors have recently proposed a new method of fault diagnosis of logical circuit by applying a pseudorandom M-sequence to the circuit under test, calculating the crosscorrelation function between the input and the output, and comparing the crosscorrelation functions with the references. This method, called MSEC method, is further extended by using a neural network in order to not only detect the existence of faults but also find the place or location of the faults. An experiment by using a simple digital circuit shows enough applicability of this method to industrial testing of circuit board.

1.Introduction

A functional logic testing of logical circuits is now an important technique, since the information devices including digital logical circuit are increasing so rapidly. For example, fault diagnosis of logical circuits boards is required in the process of producing any information devices.

There are mainly two methods in detecting faults of logical circuits. One is to analyse the circuits under test (CUT) logically and to design an optimal input sequence for CUT. D-algorithm, for example, belongs to this group. This method is called "deterministic method" and usually requires a large amount of computation time, and the design must be done for each kind of circuit.

The second method is to apply a random input to the circuit and the corresponding output is compared with the output of fault free circuit. This method is called "random testing method" and has several advantages: simple hardware, low cost and applicability to any circuits.

In this connection, we have recently proposed a new method[1] of fault diagnosis of logical circuit by applying a pseudo-random M-sequence to CUT, calculating the crosscorrelation function between the input and the output, and comparing the crosscorrelation functions with the references. This method is called M-SEquence Correlation (MSEC) method, and it has a very small probability that we overlook any faults in the circuit.

In this paper, MSEC method is further extended by using a neural network in order to not only detect the existence of faults in the circuit but also find the place or location of the faults. A simple digital circuit is taken as an example, and artificial faults are inserted to the circuit. MSEC method is then applied to this circuit to obtain the crosscorrelation functions between the inputs and outputs. Since the crosscorrelation functions contain the information about faults in the circuit, they are then applied to a neural network. After training the neural network by use of the data on the faults and resulting crosscorrelation functions, the ability of the neural network to detect the location of faults is checked.

The results of the experiment show that the trained neural network has an ability not only to detect the existence of faults but also to locate the faults in the circuits.

2.Brief description of MSEC method

The basic diagram of MSEC method is shown in Fig.1. The input to the CUT is an

n-th degree M-sequence a_i (a_i=0 or 1, i=1,2,...N, N=2^n-1) which is known as one of the pseudo-random sequences. The output sequence b_i (b_i=0 or 1) of the CUT is crosscorrelated with a_i. The crosscorrelation function between a_i and b_i is obtained as follows.

$$\Phi_{ab}(\tau) = N - 2(\sum_{i=1}^{N} a_i \oplus b_{i+\tau}) \qquad (1)$$

where $\oplus$ denotes Exclusive OR (EOR) operation and $\sum$ is the arithmetic operation. The crosscorrelation functions $\Phi_{ab}(\tau_1), \Phi_{ab}(\tau_2)$... are then compared with the correct values of $\Phi_{ab}(\tau)$'s which are the crosscorrelation functions in case of fault-free circuit. When any of $\Phi_{ab}(\tau)$ differ from the correct values, we can say that there must he some fault in the CUT.

The structure of MSEC method is simple, requiring only EOR circuit and counters. In addition to this, MSEC method has a very small probability that we miss any faults in the circuit.

The undetected fault ratio of MSEC method, that is, the expected value of the probability that we overlook any faults in the CUT, is shown to be

$$D_r \simeq \frac{2^r}{(\sqrt{\pi N})^{r+1}} \qquad (2)$$

where r is the number of delay bits we use.

The undetected fault ratio of MSEC method is shown to be much smaller than the conventional one's counting, transition counting, or even CRC(cyclic redundancy check method which is rather well known as Signature Analysis method developed by Hewlett-Packerd Co).

3.Data for training neural network

As is shown above, MSEC method has a very small probability that we miss any faults in the circuit, so it is very efficient to detect faults in a logical circuit. However, MSEC method itself cannot find the location of fault in the circuit. Since we can think that the crosscorrelation functions $\Phi_{ab}(\tau)$'s have some information on the state of the CUT, we can extract the information about the location of fault from those crosscorrelation values by applying the values of the crosscorrelation functions to a neural network. The training data for the neural network are obtained from the following experiment.

4.Experiment

As an example of CUT, a simple digital circuit (2-bit binary adder SN7482) is chosen where number of input is 5, number of output is 3.(Fig.2). In this circuit, 14 switches are inserted as the simulation of possible faults. Fig.3 shows the inserted switches (8 switches among 14 are shown), where ● shows the switch normally open, faulty when closed, and ○ shows normally closed, faulty when open.Thus up to 14 faults can be artificially made.

M-sequence of 5 degree (N=31) is applied to the input C_0, its one bit shifted veision to A_1, and likewise to B_1, B_2, A_2.

Fig.4 shows an example of the waveform of the input signal C_0 and corresponding output S_2 when there are faults at switches 1,5,6,7. The difference of the obtained crosscorrelation function and the correct crosscorrelation values is also shown in Fig.4.

Since there appears various kinds of pattern in the difference of correlation functions, we named each pattern as A,B,C.... 8 switches among 14 switches are selected and all 256 possible combinations of faults are generated artificially. For each set of possible faults, the crosscorrelation functions between 5 inputs and 3 outputs (totally 15) are calculated. Thus we obtain 256×15 patterns of correlation values, which are not always different. When we take out the case where the input is fixed to C_0, 256×3 patterns are to be obtained theoretically. But the result of the experiment showed that the number of the patterns of correlation function is less than 26×3.

These data are then applied to a neural network for training. The neural network which we have used has three layers: 78 nodes for input layer, 8 nodes for intermediate layer, and 8 nodes for output layer as is shown in Fig.5. Since the patterns of correlation values are named alphabetically, and three alphabet appears in the pattern corresponding to three outputs, the input layer requires 78 (27×3) nodes. The output layer requires 8 nodes for locating faults in one of 256 patterns of faults.

We used a neural network simulator in which up to 5 layers and up to 10,000 neurons can be simulated. After the neural network are trained by use of the training data, some patterns of fault are actually generated in the circuit and we have checked how the neural network works.

Table 1 shows an example of the result of the neural network operation. The first row of the table shows that the actual fault point is No.1, the pattern correlation functions appeared is CMD, and the neural network's response is 100% for fault 1(which coincides with the actual fault), 50% for fault 3(actually fault 3 does not exist in this case), 0% for other faults. We see from there results that the trained neural network has enough ability to find the location faults in the circuit.

5.Conclusion

A new method of fault diagnosis of logical circuit is proposed by use of pseudorandom M-sequence as its input, crosscorrelation functions between the input and output, and a neural network. This method can not only detect whether or not there exist some faults in the circuit with very small probability that we overlook any faults, but also find the location of the detected faults in the circuit. What we have to consider from now is how to reduce the number of data for training the neural network, since it will be very difficult to provide the complete training data for all possible faults in the circuit. So some sort of statistical data such as those concerning the frequently occurring fault points would be useful to reduce the training data.

References

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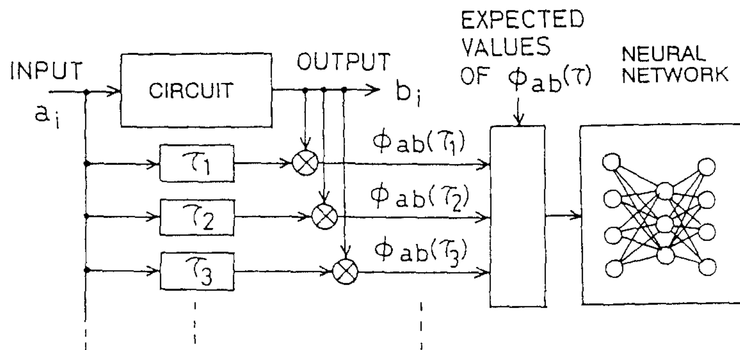

Fig.1 Basic diagram of fault diagnosis system

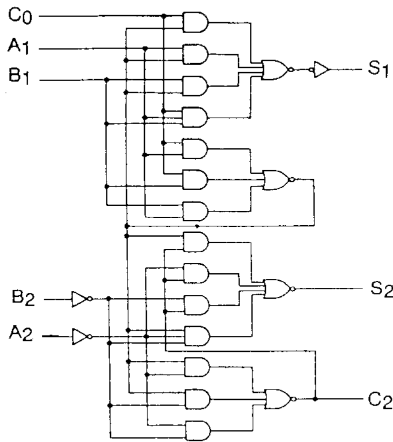

Fig.2 An example of CUT(2-bit binary full adder)

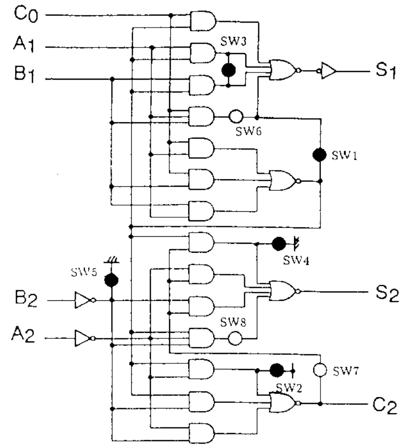

Fig.3 8 switches are inserted to CUT to simulate the possible faults

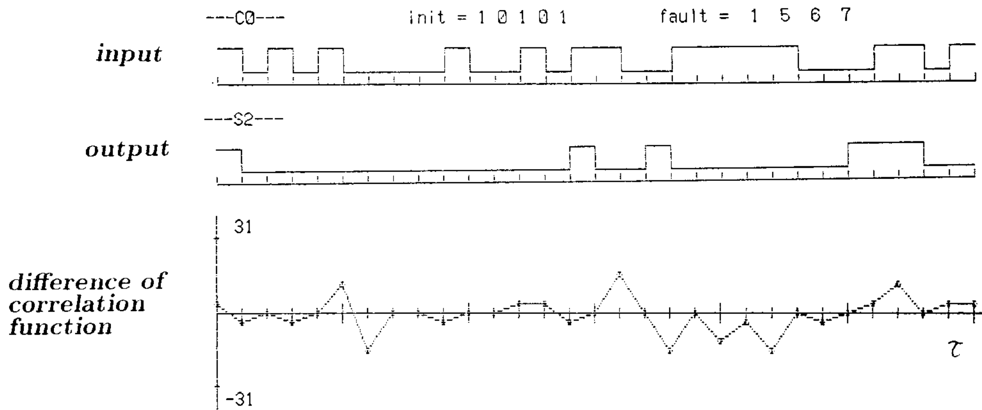

Fig.4 An example of waveform of input, output and corrrelation function

Table 1 Results of the neural network output

actual fault point	pattern of correlation function	output of neural network(%)							
		1	2	3	4	5	6	7	8
1	C M D	100	0	50	0	0	0	0	0
2	B J C	0	100	50	50	0	0	0	0
3	B C A	0	0	50	0	0	0	0	0
4	B G A	0	0	50	100	0	0	0	0
5	B E B	0	0	50	0	100	0	0	0
6	A C A	0	0	50	0	0	100	0	0
7	B B A	0	0	50	0	0	0	100	0
8	B A A	0	0	50	50	0	0	50	100
1, 7	C L D	100	0	50	0	0	0	100	0
2, 7	B B C	0	100	50	0	0	0	100	0
4, 7	B F A	0	0	50	100	0	0	100	0
5, 7	B D B	0	0	50	0	100	0	100	0
6, 7	A B A	0	0	50	0	0	100	100	0
7, 8	B A A	0	0	50	50	0	0	50	100
1, 6, 7	A L D	100	0	50	0	0	100	100	0
1, 7, 8	C A D	100	0	50	50	0	0	50	100