멀티레벨 인버터를 사용한 대용량 무효전력 보상기

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Large Scale Var Compensator Using Multilevel Inverter

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Abstract - A multilevel PWM voltage source inverter, especially five-level one, is introduced to obtain a static var compensator(SVC) as a large scale power source. In this paper, the three phase SVC is modeled using circuit DQ transformation and completely analyzed. Finally, through the experimental results from 5-kVA SVC, the validity of the analyses and the feasibility of the SVC system are shown for high power applications.

I. Introduction

It is well known that a voltage source inverter(VSI) can be used as a static var compensator(SVC) supplying fundamental reactive power.

For a large scale var compensation, however, conventional VSI's with two level outputs have their limitations to handle high power/high voltage and to operate at high switching frequency due to lack of high power self commutated semiconductor switches with high switching frequency characteristics (>1kHz). So, the high power/high voltage VSI is indispensable to large scale SVC system and the structure of the inverter primarily affects the system performance along with several control schemes.

Recently, a general circuit structure of multilevel inverter has been reported [1]. The multilevel inverter has many advantages such as better utilization of the switching devices, lower switching frequency at each semiconductor switch and reduced harmonics. Therefore, the multilevel inverter is suitable for an application to the high power/high voltage SVC system [2].

II. System Overview

Fig. 1 shows the SVC system diagram presented in this paper. The actual structure of the the five-level PWM inverter[1] is shown in Fig. 2(a) and the associated basic switching table in Fig. 2(b). Note that the voltage stress at the active switches is clamped to one capacitor voltage and thus the power devices could be fully utilized even in very high voltage range.

In particlar, for the SVC system, the multilevel inverter makes it possible to eliminate the bulky transformer which is usually required to get the appropriate input voltage at AC side of the inverter. Moreover, the circuit structure allows the five-level PWM which would result in relatively lower harmonics in the line current and thus smaller filter size.

The control target is to regulate Q_S to be zero by means of adjusting the phase angle α of the inverter with respect to that of the ac mains.

III. The Circuit DQ Transformation

Fig. 3 shows the schematic of the SVC system. Lumped resister *r* represents effective line resistance including total loss of the inverter. Assuming that harmonic components generated by switching operation are negligible, the respective existence functions for each phases of the inverter can be expressed by

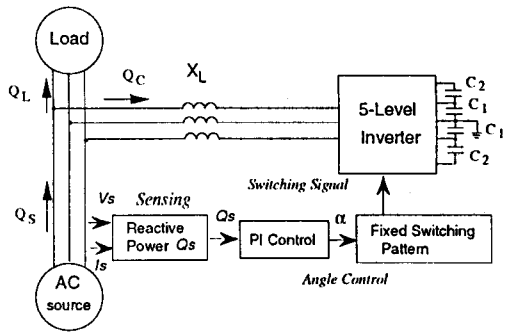
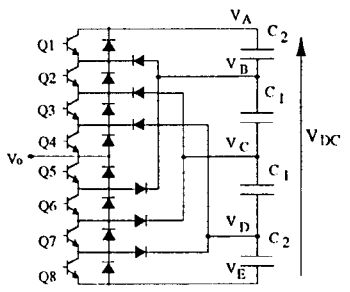


Fig. 1. Block diagram of the SVC system with five-level inverter.



V_o	V_A	V_B	V_C	V_D	V_E
Q1	1	0	0	0	0
Q2	1	1	0	0	0
Q3	1	1	1	0	0
Q4	1	1	1	1	0
Q5	0	1	1	1	1
Q6	0	0	1	1	1
Q7	0	0	0	1	1
Q8	0	0	0	0	1

1 = ON, 0 = OFF

(a) (b)

Fig. 2. (a) A pole of the five-level inverter, (b) basic switching table for the five-level inverter.

$$d_{n,a} = m_n \sin(\omega t + \alpha) \qquad (1)$$

$$d_{n,b} = d_{n,a}(\omega t - 2\pi/3), \quad d_{n,c} = d_{n,a}(\omega t + 2\pi/3)$$

with $n = -2, \cdots, 2$ where m_n and α are control variables and $m_{-1} = -m_1$ and $m_{-2} = -m_2$ from the assumption of symmetric switching of the inverter. Then, the voltage and current relationships in each sub-circuits A through C are

$$\mathbf{v}_{s,abc} = r\mathbf{i}_{abc} + \mathbf{v}_{r,abc} \quad (\text{part A}) \qquad (2\text{-a})$$

$$L\frac{d}{dt}\mathbf{i}_{abc} = \mathbf{v}_{r,abc} - \mathbf{v}_{i,abc} \quad (\text{part B}) \qquad (2\text{-b})$$

$$\mathbf{v}_{i,abc} = 2\mathbf{m}_{mod}^T \mathbf{v}_{DC}\mathbf{SIN}(\omega t + \alpha) \quad (\text{part C}) \qquad (2\text{-c})$$

$$\mathbf{i}_{DC} = \mathbf{m}_{mod}\mathbf{i}_{abc}^T \mathbf{SIN}(\omega t + \alpha) \quad (\text{part C}) \qquad (2\text{-c})$$

where

$$\mathbf{SIN}(\omega t + \alpha) = \begin{bmatrix} \sin(\omega t + \alpha) \\ \sin(\omega t + \alpha - \frac{2\pi}{3}) \\ \sin(\omega t + \alpha + \frac{2\pi}{3}) \end{bmatrix}, \qquad \mathbf{i}_{abc} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

$$\mathbf{v}_{s,abc} = \begin{bmatrix} v_{sa} & v_{sb} & v_{sc} \end{bmatrix}^T = \sqrt{2/3} \cdot \mathrm{V_s} \cdot \mathbf{SIN}(\omega t)$$

$$\mathbf{v}_{r,abc} = \begin{bmatrix} v_{ra} & v_{rb} & v_{rc} \end{bmatrix}^T, \quad \mathbf{v}_{i,abc} = \begin{bmatrix} v_{ia} & v_{ib} & v_{ic} \end{bmatrix}^T$$

$$\mathbf{v}_{DC} = \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}, \quad \mathbf{i}_{DC} = \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}, \quad \mathbf{m}_{mod} = \begin{bmatrix} m_1 \\ m_2 \end{bmatrix}.$$

Then, three phase time-varying nature of the fundamental circuit can be eliminated by employing the appropriate synchronously rotating transformation matrix, K. The power invariant DQ tranformation matrix K is given by

$$\mathbf{K} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\omega t + \alpha) & \cos(\omega t + \alpha - 2\pi/3) & \cos(\omega t + \alpha + 2\pi/3) \\ \sin(\omega t + \alpha) & \sin(\omega t + \alpha - 2\pi/3) & \sin(\omega t + \alpha - 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}$$

where $\mathbf{x}_{qdo} = \mathbf{K}\mathbf{x}_{abc}$ and $\mathbf{K}^{-1} = \mathbf{K}^T$.

Applying the matrix K to each system variable yields the following equations:

$$\mathbf{v}_{s,qdo} = r\mathbf{i}_{qdo} + \mathbf{v}_{r,qdo} \quad (\text{part A}) \qquad (3\text{-a})$$

$$L\frac{d}{dt}\mathbf{i}_{qdo} = \mathbf{v}_{r,qdo} - \mathbf{v}_{i,qdo} \quad (\text{part B}) \qquad (3\text{-b})$$

$$\mathbf{v}_{s,qdo} = 2\eta\mathbf{D}^T\mathbf{v}_{DC} \quad (\text{part C}) \qquad (3\text{-c})$$

$$\mathbf{i}_{DC} = \mathbf{D}\eta^T\mathbf{i}_{qdo} \quad (\text{part C}) \qquad (3\text{-d})$$

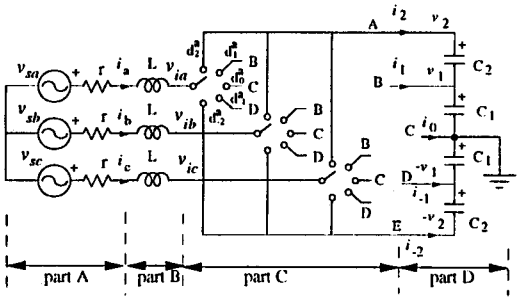


Fig. 3. The schematic of five-level inverter.

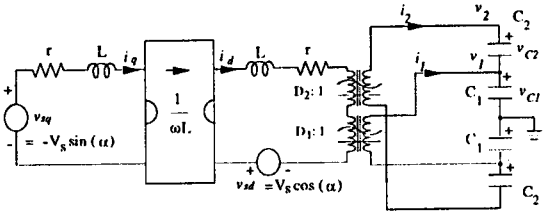


Fig. 4. Circuit DQ transformed circuit of the SVC system

where, $$\mathbf{D} = \begin{bmatrix} D_1 \\ D_2 \end{bmatrix} = \sqrt{\frac{3}{2}}\begin{bmatrix} m_1 \\ m_2 \end{bmatrix}, \qquad (4)$$

$$\mathbf{v}_{s,qdo} = \mathrm{V_s}\begin{bmatrix} -\sin(\alpha) \\ \cos(\alpha) \\ 0 \end{bmatrix}, \quad \mathbf{Z}_s = \begin{bmatrix} 0 & -\omega L & 0 \\ \omega L & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \quad \eta = \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix}.$$

Using (3) and (4), the equivalent circuit can be reconstructed as shown in Fig. 4.

In the steady state operation, the inductors seem to be short and the capacitors open since all of the DQ circuit variables imply DC values. Thus, using the DC circuit as shown in Fig. 5, the characteristics of the SVC in the steady state can be obtained without combersome equational manipulations. From Fig. 5,

$$V_{sq} = -V_s \sin(\alpha), \qquad V_{sd} = V_s \cos(\alpha) \qquad (5)$$

$$I_q = V_{sq}/r = -V_s \sin(\alpha)/r, \qquad I_d = 0.$$

Therefore, the reactive power Q_C and the real power P_C drawn by the inverter is expressed by

$$Q_C = V_{sq} I_d - V_{sd} I_q = \frac{V_s^2}{2r}\sin(2\alpha) \qquad (6)$$

$$P_C = V_{sq} I_q + V_{sd} I_d = \frac{V_s^2}{r}\sin^2(\alpha) \qquad (7)$$

Supposing the balanced voltages of each DC side capacitors, the resultant operating DC side voltage V_{DC} can be found from Fig. 5 as follows:

$$V_{DC} = \frac{V_s}{D_2 + D_1/2}\left\{\cos(\alpha) - \frac{\omega L}{r}\sin(\alpha)\right\} \qquad (8)$$

If we have $f = 60\ Hz$, $L = 5\ mH$, $r = 0.5\ \Omega$, $V_s = 6600$ V, $m_1 = m_2 = 0.3$ and a maximum of $\alpha = 5^o$, then, employing 4.5kV/3kA GTO's, the generated reactive

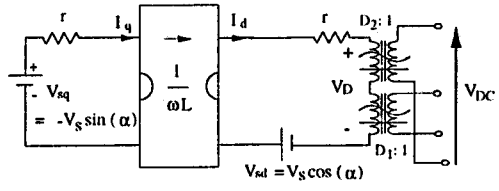
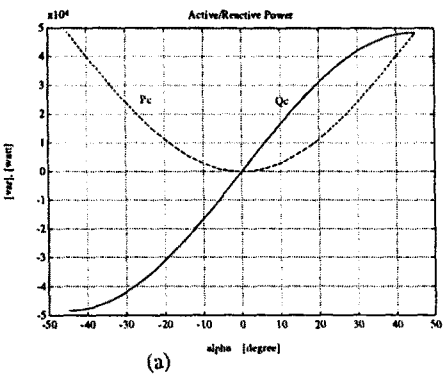
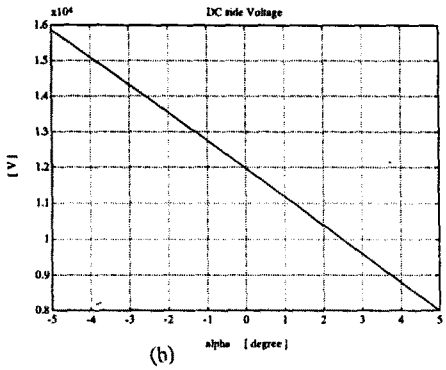


Fig. 5. DC circuit for steady state analysis



(a)



(b)

Fig. 6.(a) Qc and Pc vs. α, (b) V_{DC} vs. α

power of 7.5 Mvar would be achieved with the maximum DC side voltage of 8 kV and thus 2 kV at each DC capacitors while requiring no coupling components such as transformers. Fig. 6(a) and Fig. 6(b) show the magnitude of Q_C and P_C and V_{DC}, respectively, as a function of α with the aforementioned circuit conditions.

IV. Experimental Results

To confirm the feasibility of the suggested var compensation system, experimental transisterized prototype of 5 kVA is implimented and tested.

Fig. 7 shows the ac line current i_a and the output phase voltage v_{in} of the inverter generating capacitive var. From Fig. 7, it can be seen that the DC capacitor voltages are balanced, resulting in the same hights in step changes.

Fig. 8 shows the closed loop responses for step change in var command from inductive to capacitive. It is rather simple to design a PI controller for the SVC system cpmpletely modeled to get the rise time of 30 *msec* and thus the bandwidth of 10 *Hz* as shown in Fig. 8.

V. Conclusion

For a large scale var compensation, a multilevel PWM voltage source inverter, especially five-level one, is introduced and then analyzed using circuit DQ transformation. The experimental verifications show the validity of the modeling and analysis and feasibility of the var compensation system for high power/high voltage applications.

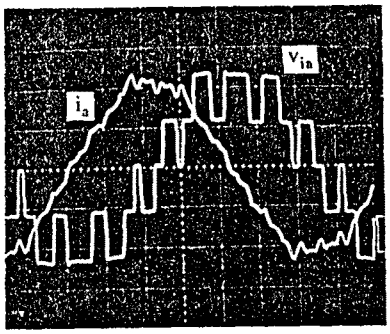


Fig. 7. Experimental waveforms of the output phase voltage and line current for leading var compensation. (100V/div, 5A/div, 2msec/div)

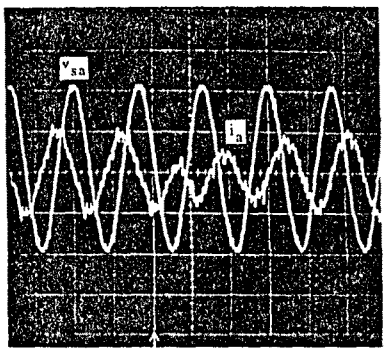


Fig. 8. The oscillograms of closed loop response to step reversal of var command from capacitive var to inductive var, (90V/div, 10A/div, 10msec/div).

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