12

Three Dimensional Analysis of Device Cell Structure

Hyung-Ho Park, Hyung-Mun Kim, Hee-Tae Lee, Sahn Nahm, Sang-Gi Kim, Joong-Whan Lee, Byong-Hwa Koak, Kyoung-Ik Cho and Young-Il Kang

Semiconductor Technology Division, ETRI, Taejeon, Korea

Cell structure of Complementary Metal Oxide Semiconductor (CMOS) device with 1 μm design rule has been analyzed using Secondary Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), X-ray Photoelectron Spectroscopy (XPS), Auger Electron Spectroscopy (AES) and Secondary Ion Mass Spectrometry (SIMS).

Specimens with 2 mm x 3 mm dimensions have been prepared using ultrasonic disc cutter which is normally used for TEM specimen preparation, from a capsuled chip with 1 cm x 1 cm dimension. XPS analysis showes that the surface passivation layer is composed of silicon nitride. Cross - sectional SEM specimens in the two different directions have been prepared by fine polishing and selective etching (Fig. 1). SEM analyses have been done after every polishing step of 2 μm. Through these analyses, cell structure and its physical parameter have been extracted. This cell is found to be 1.0 μm CMOS with a triple metal structure. The implanted areas for source / drain have been also clearly observed (Fig. 2). Barrier metal and constituents of metal layers have been revealed by AES and TEM / Energy Dispersive X-ray (EDX) analyses. SIMS analysis has shown that BPSG is used for planarization.

Through the above analyses, estimated process for the device fabrication can be also drawn. This interpretation work can be also applied to a failure analysis of Integrated Circuits (IC).

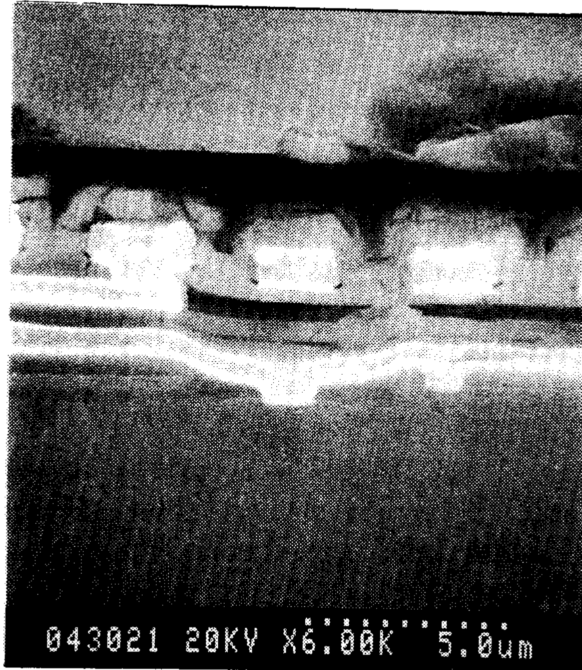

Fig. 1 Cross - sectional SEM image showing triple metal structure after selective etching for 15 seconds

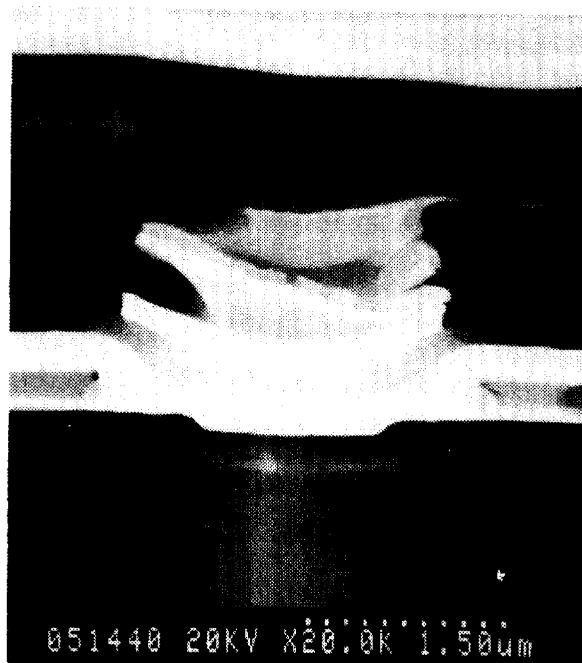

Fig. 2 Cross - sectional SEM image of n^+ source / drain region after selective etching for 40 minutes