'95 KACC (1995. 10. 23 ~ 25)

Output Power Maximizing in Ultrasonic Transducer Driven at 1 MHz Utilizing Auto-tune MOS-FET RF Inverter

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Abstract When the ultrasonic transducer operating at 1 MHz for use in cleaning semiconductor wafers or other industrial materials is driven from the MOS-FET DC-to-RF inverter, the output power severely depends on the frequency of operation since the quality factor of the transducer is high. In order to tune to the resonating frequency of the ultrasonic transducer, the drive signal frequency of the MOS-FET power inverter is automatically scanned until the frequency is set at the resonating frequency of the ultrasonic transducer. A PLL is used to set the frequency at the resonating point so that the output power of the ultrasonic transducer is maximized. The control circuit consists of an output power sensing circuit, a PLL controller, a frequency standard, and other peripheral circuits. The operation was satisfactory when the transducer having an output of 600 W at 1 MHz was used.

Keywords Ultrasonic transducer, MOS-FET, Inverter, PLL, Resonating frequency

1. INTRODUCTION

Shortwave MOS-FET DC-to-RF inverters have been constructed for use in various applications[1]-[3]. These inverters are mainly used to drive the resonating load. Among the drives for these resonating loads, the ultrasonic transducer drive is one of the most interesting topics. The ultrasonic transducer is used for cleaning the surfaces of the materials, i.e. semiconductor materials or glasses. In general, the ultrasonic transducers have specific resonating frequencies, and at those resonating frequencies, the input power of the ultrasonic transducer might be maximized[4]. When the voltage is in phase with the current, the safety operation area of the MOS-FET may be maximized. However, the manual tuning to the exact resonating frequency is not so easy when accomplished using the variable resister.

This paper describes the optimization of the operation of the MOS-FET DC-to-RF inverter using the phase-locked loop (PLL) circuit to automatically tune to the resonating frequency of the ultrasonic transducer.

On basis of the impedance change with frequency, the operating frequency range of the VCO used to determine the operating frequency of the MOS-FET DC-to-RF inverter can be set using the PLL circuit.

Before the construction of the experimental setup, the equivalent circuit parameters are used to determine the operating point of frequency for the MOS-FET DC-to-RF inverter so that the PLL circuit parameters to specify the resonating characteristic can easily be specified by the resonating circuit determined by equivalent circuit parameters.

2. SCHEMATIC DIAGRAM

Figure 1 shows the schematic diagram of the auto-tune inverter circuit. This system consists of a voltage controlled oscillator (VCO), flip-flops, a MOS-FET inverter, an ultrasonic transducer, and a phase comparator. The VCO and the phase comparator are housed in a package as a PLL IC, the VCO generates the basic drive signal of approximately 4 MHz, and the signal is counted down to a quarter by a pair of flip-flops. The one of output signals of the flip-flops at approximately 1 MHz (4 MHz / 4 = 1 MHz) is fed to the MOS-FET RF inverter circuit through the buffers. The output voltage of the inverter drives the ultrasonic transducer. The another output signal of the flip-flops is fed to the phase comparator. The current signal of the transducer is also fed to the phase comparator. Using the phase comparator, a pair of signals are compared each other in phase, then the result of the comparison is fed back to the VCO to control the generating frequency.

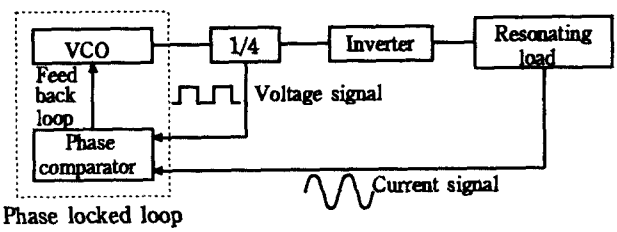

Fig.1. Schematic diagram of the auto-tune inverter circuit.

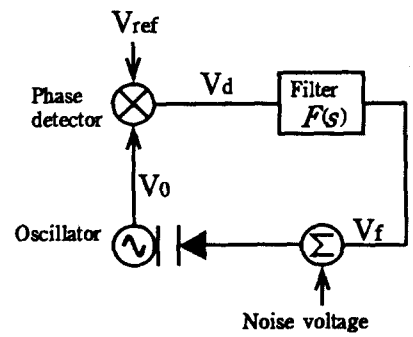

Fig.2. Block diagram of the phase-locked loop.

3. OPERATION OF PLL CIRCUIT

A. Theory[5]

The purpose of the PLL is simply to keep the two oscillators, on the average, in phase quadrature. When the oscillator output phases are nearly in phase quadrature, the output voltage of the phase detector is proportional to the difference in phase between the two output signals.

The block diagram for the PLL is shown in Figure 2. The noise voltages which are summed into the loop are in a schematic way of representing $\phi_n(t)$, the open-loop phase noise of the oscillator. The phase noise in the reference oscillator is denoted as $\phi_{ref}(t)$.

The analysis of the PLL yields such a result as

$$\phi_0(s) = \phi_n(s)\left[\frac{1}{1+G_{eq}(s)}\right] + \phi_{ref}(s)\left[\frac{G_{eq}(s)}{1+G_{eq}(s)}\right] \quad (1)$$

where $Geq(s)$ is the open loop transfer function defined by

$$G_{eq}(s) = \frac{K_0 K_d F(s)}{s} \quad (2)$$

and $\phi_n(s)$ and $\phi_{ref}(s)$ are the Laplace transforms of the corresponding time-varying quantities. K_0 and K_d are the gain constants of the VCO and of the phase comparator, respectively. The output voltage of the phase detector can be calculated as,

$$V_d(s) = \frac{K_d\left[\phi_{ref}(s) - \phi_n(s)\right]}{1+G_{eq}(s)} \quad (3)$$

The feed back voltage V_f to the VCO is then given by,

$$V_f(s) = F(s)V_d(s)$$

$$= \frac{sG_{eq}(s)}{G_{eq}(s)}\left[\phi_{ref}(s) - \phi_n(s)\right] \quad (4)$$

Thus, the oscillation frequency of the VCO can be controlled.

B. Operation

Figure 3 shows the block diagram of the PLL IC. In Figure 3 , R_1, R_2, and C_1 decide the oscillation frequency range of the VCO. The phase comparator is the phase and frequency detector of positive edge trigger type.

Figure 4 shows the waveforms of the PLL IC. Figure 4(a) shows the case that the PCAin signal is advanced to PCBin signal, and Figure 4(b) shows the case the PCAin signal is delayed from the PCBin signal. In Figure 4(a), the output voltage VCOin becomes high, so that the oscillation frequency of the VCO goes high. On the other hand , in Figure 4(b), the output voltage VCOin becomes low, so that the oscillation frequency of the VCO goes low.

4. EXPERIMENTAL STUDY

This section makes it sure that the operation of the PLL circuit is used for making the VCO tune to the resonating frequency of the load at low frequency

A. Setup

Figure 5 shows the experimental circuit configuration. The circuit consists of a PLL circuit, a pair of flip-flops, a complementary switching circuit, and a resonating load. The input voltage to the system is set at 5 V in high state, so that the VCO control voltage is in range of 0 V to 5 V. The oscillation frequency range of the VCO in PLL circuit is 25 kHz to 70 kHz. After counted down, the input frequency to the switching circuit becomes approximately 7 kHz to 18 kHz. The resonating load has a resonating frequency of approximately 12 kHz.

The frequency set when the voltage waveform is in phase with the current waveform is the resonating frequency of the load.

Figure 6 shows the resonating load circuit configuration. This load has three states of resonating frequencies. The resonating frequency of the load is given by equation (5).

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (5)$$

This load is changeable in resonating frequency by switching SW_1 and / or SW_2. When both SW_1 and SW_2 are off, $C=C_2$ and then the resonating frequency of the load becomes 15.3 kHz. When SW_1 is on while SW_2 is off, $C=C_1+C_2$, then the resonating frequency of the load becomes 11.5 kHz. When both SW_1 and SW_2 are on, $C=C_1+C_2+C_3$ then the resonating frequency of the load becomes 9.8 kHz.

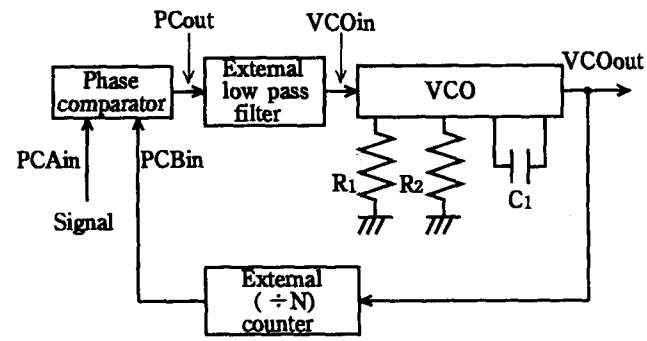

Fig.3. Block diagram of the PLL IC.

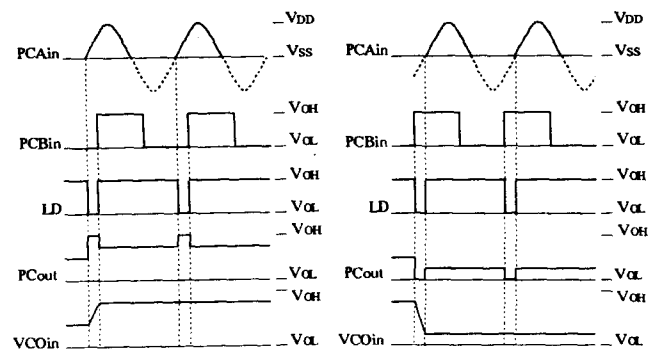

Fig.4. Time chart of the PLL.
(a) When PCAin is advanced to PCBin.
(b) When PCAin is delayed from PCBin.

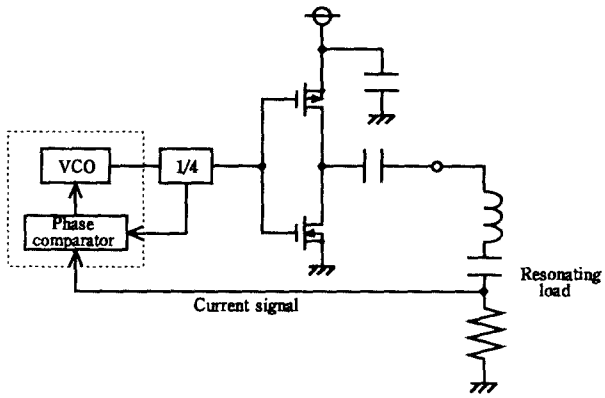

Fig.5. Experimental circuit configuration.

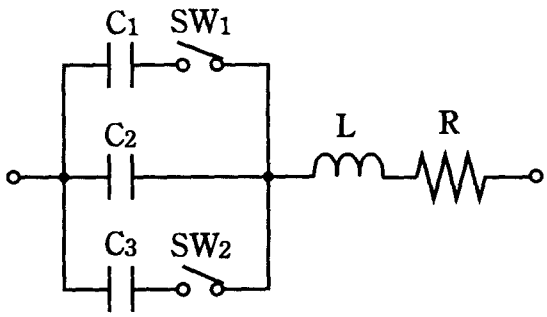

Fig.6. Resonating load.

B. Operation

Three operation modes of the system is summarized on Table 1. The VCOin voltage is changeable by the resonating frequency of the load. This is the way that the VCO output frequency is controlled.

Table 1. Three operation modes of the PLL.

Resonating frequency	VCOin voltage
9.8 kHz	2.95 V
11.5 kHz	3.37 V
15.1 kHz	4.50 V

Figure 7 through Figure 9 show the waveforms of the input signals to the phase comparator. In Figure 7, the frequency is set at 9.8 kHz, in Figure 8, the frequency is set at 11.5 kHz, and in Figure 9, the frequency is set at 15.1 kHz. In Figures 7 through 9, (a) indicates the output voltage waveform of the flip-flops, and (b) indicates the current waveform of the resonating load. In all cases, the voltage phase is in phase with the current phase.

Figure 10 shows the signal waveforms of the PLL circuit operating at 11.5 kHz. Figure 10(a) shows the output signal of the flip-flops, and Figure 10(b) shows the phase comparator output signal waveform. The pulse voltage which checks the shift between the two signals can be seen.

5. OPERATION USING ULTRASONIC TRANSDUCER

Figure 11 shows the equivalent circuit configuration of the real ultrasonic transducer operating at 1 MHz. By using the current probe, it is possible to check the current signal.

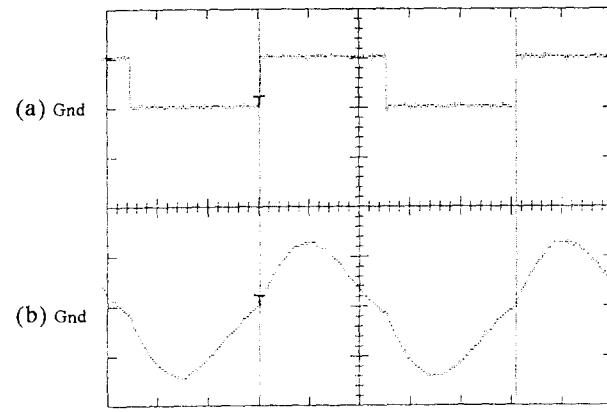

Fig.7. Input signal waveforms at 9.8 kHz.
(a) Output voltage waveform of the flip-flop.
H : 5 V/div, V : 20 μs/div.
(b) Current signal waveform.
H : 2 V/div, V : 20 μs/div.

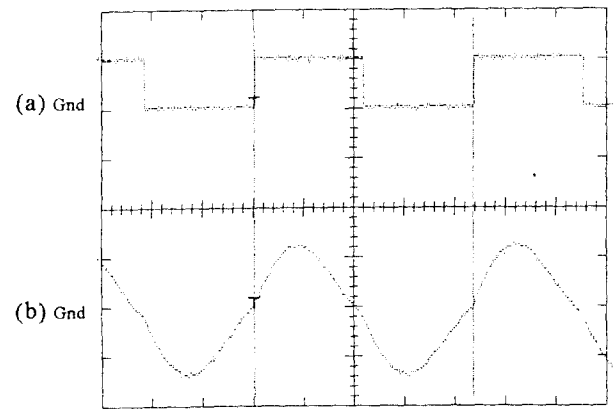

Fig.8. Input signal waveforms at 11.5 kHz.
(a) Output voltage waveform of the flip-flop.
H : 5 V/div, V : 20 μs/div.
(b) Current signal waveform.
H : 2 V/div, V : 20 μs/div.

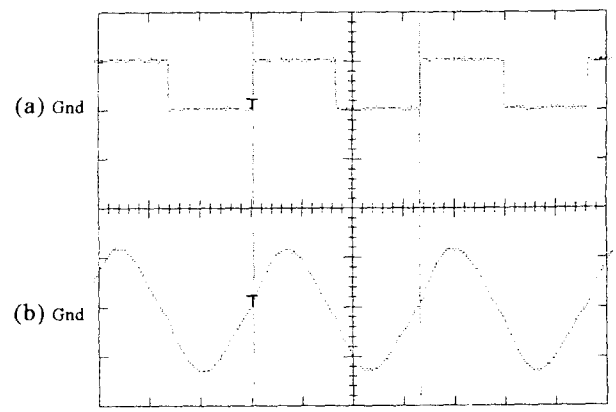

Fig.9. Input signal waveforms at 15.1 kHz.
(a) Output voltage waveform of the flip-flop.
H : 5 V/div, V : 20 μs/div.
(b) Current signal waveform.
H : 2 V/div, V : 20 μs/div.

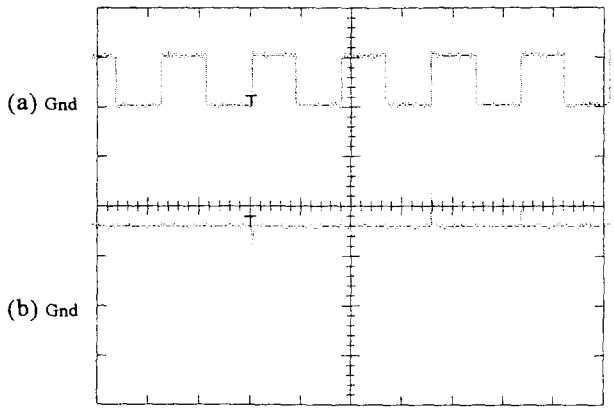

Fig.10. Output signal waveforms of the PLL.
(a) Output voltage waveform of the flip-flop.
H : 5 V/div, V : 50 μs/div.
(b) Phase comparator output signal.
H : 2 V/div, V : 50 μs/div.

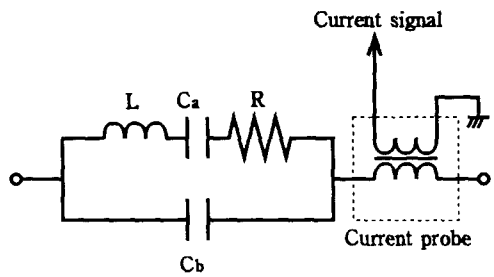

Fig.11. Equivalent circuit configuration of the ultrasonic transducer.

6. CONCLUSION

The PLL circuit is used to automatically tune to the resonating load frequency, and its operation is confirmed to be satisfactory.

In the real ultrasonic transducer, sensing the current signal is difficult because the transducer has ultralow resonating impedance. However, if the current probe is used, it would be possible to sense the current without shifting its phase. This system is useful to tune to the operating frequency of the ultrasonic transducer for the cleaning by appropriately setting the oscillation frequency range of the VCO.

This system was confirmed to be useful to the real ultrasonic transducer at 1 MHz on the experimental study at low frequencies.

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