

Fabrication of Silicon Field Emitter Array with a Focusing Electrode by Chemical-Mechanical-Polishing Process

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Field emitter arrays (FEAs) are extensively studied for electron sources in vacuum microelectronic devices and field emission display [1]. FEAs generating focused electron beams have been much attention [2]. In conventional silicon FEAs fabrication, an electron beam deposition and lift-off process, and a photo resist etch-back process were used. The former causes some problems such as high leakage current, gate hole asymmetry and gate diameter enlargement [3], while the latter also has a demerit of unclear-cutted gate due to the etch-back process [4]. In order to overcome these problems, we have fabricated silicon tips using Chemical-Mechanical-Polishing (CMP) process for the formations of gate electrode and focusing electrode.

The fabrication sequence of silicon FEAs was illustrated in Fig. 1. The starting materials were n-type silicon wafers with a resistivity of 5~8 Ω -cm. An n-well was formed by high dose ($5 \times 10^{15}/\text{cm}^2$) ion implantation of phosphorus and then a thermal oxide was grown. This oxide layer was patterned for an etch-mask with an optical stepper, resulting in a disc of 1.2 μm in diameter. The silicon was isotropically etched using SF_6 gas and then anisotropically etched using $\text{SF}_6 + \text{O}_2$ gases to increase the emitter tip height for a given disc size. Then, a high temperature oxidation was carried out to sharpen the silicon tips. After etching the etch-mask oxide and thermal oxide, an oxide film of 7000 \AA was deposited by LPCVD for the gate dielectric material. Polysilicon for the gate electrode was deposited and doped with POCl_3 at 900 $^\circ\text{C}$. The CMP process was used for the gate electrode formation by partial polishing the polysilicon gate above the tip. In the CMP process, the gate rim shape depends on the polishing time and pressure during the polishing. The etch rate of the polysilicon was about 2300 $\text{\AA}/\text{min}$ at 5 psi of polishing pressure. The etch selectivity between polysilicon and the oxide was larger than 200:1. We have chosen Naico 2371 as a polishing slurry due to its large etch selectivity, and polishing pad was a stack of IC1000 / Suba IV. For the focusing electrode, the second oxide and polysilicon were deposited sequentially. With polishing the second polysilicon layer followed by a HF dipping process, FEA tips with focusing electrode could be produced.

Fig. 2 shows a SEM photograph of the fabricated tips array with extracting and focusing electrodes. The lower gate with a 2 μm -diam opening act as an extraction electrode controlling the emission current, and the upper one with a 3 μm -diam opening acts as an electrostatic lens focusing the electron trajectories. The focusing electrode is located above the first gate electrode by 0.8 μm . Electrical measurements were carried out in an UHV chamber after removal of native oxide on the silicon tip surface by a HF dip. Fig. 3 (a) shows the anode and the gate currents from the 2809 tips array without focusing electrode. The turn-on gate voltage was about 50 V. The anode current from the tips array was 31 μA at a gate voltage of 80 V, corresponding to 11 nA from the each tip, while the gate current was remained less than 0.1% of the anode current. Fig. 3 (b) shows the Fowler-Nordheim (F-N)

plot of the emitted anode currents for the sample. The F-N plot shows typical field emission characteristics. Vertical type focusing electrode structures could be easily obtained by using the CMP process. The vertical type electrode is effective for focusing the emitted electrons from emitter [2]. The measured focusing effect will be shown in the conference.

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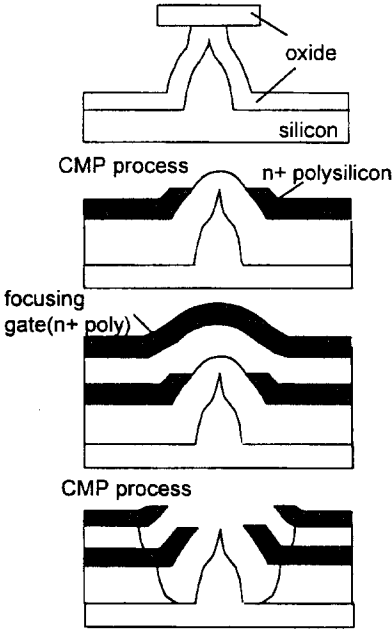


Fig.1 Fabrication sequence of silicon FEAs with focusing electrode by CMP process.

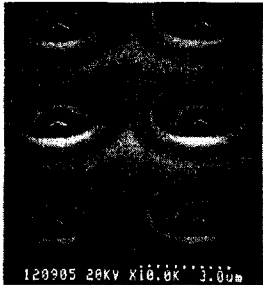


Fig.2 SEM photographs of FEA with focusing electrodes by CMP process.

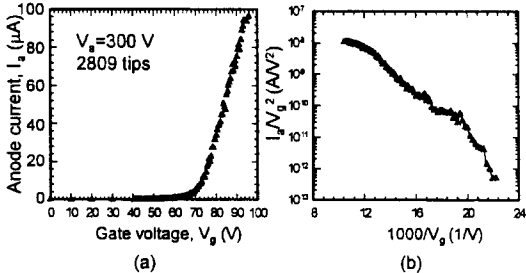


Fig. 3 Emission characteristics of a FEA with 2809 tips. (a) I_a - V_g characteristics (b) F-N plot of the anode current