SIMULATION OF POWER ELECTRONIC CIRCUITS

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INTRODUCTION

Power electronic engineers want power electronic devices with higher ratings like the maximum blocking voltage and the turn–off current capability on the one hand or higher switching frequency on the other hand. The first objective avoids series and parallel connections of the devices when the power rating is increased. The second objective results in a lower harmonic content and thus a reduction of the filtering.

However it was a widely accepted fact, that increasing the power rating — for example a higher blocking voltage or a higher turn–off current capability or reducing the on–voltage — results in higher switching losses and this leads to a decrease of the switching frequency as long as the same technology for the devices is used.

There have been different approaches in the past to avoid the undesired couplings of the mentioned objectives. The first approach was the development of various snubber circuits. The second approach was the development of the resonant topologies for power electronic circuits. Both proposals however result in additional components, that in turn leads to a higher complexity of the power electronic circuits from both the operating and the mechanical design point of view. Furthermore often the maximum stress on the devices will increase — which again is undesirable. A third approach is to change the design of the power electronic devices itself. There has been a fundamental idea to combine unipolar and bipolar design solutions. Such combinations of design solutions should enable us to incorporate the power ratings of the bipolar devices with the low control expense of the unipolar devices in the gate unit. But most of these device designs had to cope with repetitive cell structures which can result in current pinching especially during fast switching–off transients or a parasitic thyristor structure in the power path with the risk of latching.

The paper will concentrate on new solutions like the "hard driven GTO", the IGCT (Integrated Gate Commutated Thyristor) or Trench elements. Due to these new devices new areas for power electronics can be considered such as medium voltage electrical ac–drives or "Flexible AC–Transmission Systems" (FACTS). These new areas generally have high power ratings and experimental investigations are time consuming, difficult and costly. Therefore "Computer Aided Engineering" (CAE) is an advantageous solution for the analysis, synthesis and optimization of such power electronic circuits and in general.

EMERGING POWER ELECTRONIC DEVICES

As mentioned in the first chapter, there was a continuous effort to improve the characteristics of the power electronic devices themselves. The first research activity was the variation of the design, a well–known example is the IGBT. An emerging device will be the GCT soon and perhaps in the near future the Trench–elements. Another option are new materials like GaAs and more favorably SiC.

First we have to consider in a retrospective the accepted GTO characteristics in the past [1]–[7] to understand the objectives of the hard driven GTO and GCT.

During the last years a saturation in the device specifications was achieved. It is due mainly to its transient behavior [8]:

- The turn–on process is completely non–homogeneous: After the firing of some spots (within few cells) the plasma has to spread sideways throughout the whole wafer. The lateral spreading time constrains anode current rise time to $dI_A/dt \leq 500\ A/\mu s$. Higher gradients may overload the early conducting cells and destroy the device. The current rise–time limitation is realized through big snubbing inductances.
- In order to achieve a reasonable turn–off gain of 3–5 [9], a comparatively slow gate current rise with respect to GTO's response time is applied. This is followed by large storage times ($\sim 20\ \mu s$), non–homogeneous turn–off transient, limited dV/dt and the stringent need for bulky snubbing capacitors.

Therefore, the converter is dominated by voluminous passive components, inductors, capacitors and resistors. With conventional topologies, most of the switching losses occur in the snubber and only a small part are generated in the GTO itself.

On the other hand experimental investigations with high voltage FCTh structures [10] proved that advanced switching capabilities and homogeneous switching behavior of the device is obtained by fast, powerful and accurate control. These research results have been the starting point of the development of the hard driven GTO and in a further step to the GCT and were reported in [11].

There are other interesting developments for emerging power electronic devices; an overview is given in [13]. Such emerging devices can be the Trench–elements. An existing device is the Trench–IGBT. A comparison of a Planar– and a Trench–IGBT is shown in fig. 1.

Obviously there are several advantages when comparing the structures of both devices. First the additional resistor R_{jFET} between the p–wells of the cells is eliminated with the Trench–structure. Secondly the size of a cell in the Trench–IGBT is considerably smaller than in the Planar–IGBT and thirdly the undesired parasitic n–p–n–transistor which is responsible for latch up is less

effective due to the gate structure in a Trench–IGBT. Disadvantages to some extent are the more complex design (limiting electrical field effects) and process technology (Trench–gate) of the Trench–IGBT.

Additional options for the Trench–devices are to switch these devices from bipolar to unipolar current conduction and vice versa to achieve for example much improved switching transients for a Trench–diode [13].

In the future there will be a further option of new materials like SiC. Again an introduction to this new material is given in [13]. Favorable characteristics are the wide band gap, the high breakdown electrical field and a high thermal conductivity. There are different figures of merit like the figure of merit from Johnson (JFM [22]), Baliga (BFM, [24]) and Schlangenotto (SFM, [25]), which estimate the advantage of SiC against Si for example. More recent investigations [26] show a more precise picture. First results are published in [23] for diodes.

PHYSICAL MODELS FOR POWER SEMICONDUCTORS

If circuit simulation of power electronics is considered, there are different proposals for the models of the components. Especially there is a wide range of models for the power semiconductors. On the one hand Spice-models are often proposed because these models can run on a PC and the duration of the simulation of power electronic circuits is short. However, there is one essential drawback: the switching behaviour of the power semiconductors neglects the influence of the low doped zone(s) with normally high level injection, which is one of the main characteristics of the power semiconductor. These Spice-models are based on signal processing devices and these components do not include low doped zone(s). Therefore these Spice-models cannot be used to design power electronic topologies.

Due to this disadvantage the original Spice-models had been expanded to show such principle effects like the reverse recovery. But in these expanded Spice-models the interesting effects are normally implemented in the original Spice-models with additional electronic circuits to mimic the desired effect. Therefore the desired effect is only imitated in a generally narrow area of operating points. Consequently such solutions are not very well suited for a general circuit simulation with different power semiconductor topologies and in a very wide operating range of the power semiconductors.

Another quite different approach is the device simulation (one-, two- and three-dimensional for each power semiconductor like Pisces, DESSIS or Medici). This approach shows the behavior of power semiconductors in detail, which result from the four coupled equations (transcendent differential equations):
Poisson's equation:

$$\nabla D = \rho(x,y,z) \tag{1}$$

Current density equations:

$$Jn = q \cdot \mu_n \cdot E \cdot n + q \cdot D_n \cdot \nabla n \tag{2}$$

$$Jp = q \cdot \mu_p \cdot E \cdot p - q \cdot D_p \cdot \nabla p \tag{3}$$

Continuity equations:

$$\frac{\delta n}{\delta t} = -Rn + \frac{1}{q} \cdot \nabla J_n \tag{4}$$

$$\frac{\delta p}{\delta t} = -Rp + \frac{1}{q} \cdot \nabla J_p \tag{5}$$

Additionally we have to consider the ambipolar differential equation (ADE), which is necessary to describe the charging and decharging in the intrinsic or low doped zone(s).

This equation arises from the elimination of the electric field E with p = n in the current equations and the insertion of the resulting ambipolar current density equation for Jp into the continuity equation for p.

$$\frac{\delta p}{\delta t} = \frac{\delta D}{\delta x} \cdot \frac{\delta p}{\delta x} \cdot D \cdot \frac{\delta^2 p}{\delta x^2} + \frac{J}{q} \cdot \frac{1}{(b+1)^2} \cdot \frac{\delta b}{\delta x} - R \tag{6}$$

$b = \frac{\mu_n}{\mu_p}$: mobility ratio

$D = \frac{2 \cdot \mu_n \cdot \mu_p}{\mu_n + \mu_p}$: ambipolar diffusivity

$R = \frac{p}{\tau_{SRH}} + C_A \cdot p^3$: composite recombination rate

Since D, b, τ_{SRH} are functions of the local carrier density, the local dopant density and other local parameters, these quantities are also functions of space.

However such simulations are complex, need a powerful CPU and are CPU-time consuming; besides the number of power semiconductors during one simulation is limited. Due to these results a special solution for the modeling of power semiconductors — the physical modeling was used for all power semiconductors as e.g. the main switches like the GTO, IGBT or MOSFET, the freewheeling and snubber diode [27], [28].

Physical models start from the geometric structure of the power semiconductors considered, use the semiconductor equations above to cover all physical effects and use the parameters like the geometric data or the doping profiles. But the semiconductor equations result in a set of transcendent equations, which cannot be solved directly. The second decision in the development of physical models was to accept a one-dimensional geometric approach. This decision is especially acceptable for hard driven semiconductors in a very wide range of operating points and applications. But even if only a one-dimensional approach is used, the set of equations remain transcendent. The third decision in the process of the modeling depends on the desired accuracy of the simulation especially during the switching transients. It is well-known, that the low doped zones normally reach the high injection level during the on-state. Due to this effect, the ambipolar diffusion equation is solved very precisely with a specific approach in our models, to achieve accurate simulations of the transients.

In fig. 2 the structure of the model of the power diode and in fig. 3 the GTO structure is shown. The structure of the diode in fig. 2 has only one low doped zone, but the GTO has a low doped p- and n-base. In these low

doped zones the ambipolar equation is solved like in device simulation programs by a segmentation of the zone which is time- and position-variant; so with a limited number of segmentations a result with high accuracy is achieved for the low doped zone. The high doped zones are approximated by more simple concentrated models [29], [30]. Due to this approach these physical models cover a very wide range of operating points and applications. To reduce the efforts for simulations these physical models of the semiconductors were implemented in a network simulator - in this case SABER. This results in a short netlist of the topology of the power electronic circuit on he one hand and the device-parameters of the power semiconductor on the other hand.
These advantageous features of the physical models for power semiconductors [28], [29], [30] enable the research and development in the industry to use CAE simulation instead of only hardware experiments.

In fig. 4 comparisons of experimental results and simulations at the same temperature and operating point are shown. It can be seen that the experimental result and the simulation have a very close correlation, considering the existent parameter variations in the devices, which are not known exactly. The models had been validated by simulating different topologies like choppers with different snubbers, choppers using the active semiconductor as ZVS or ZCS and in a temperature range from 400 K - 100 K, comparing the simulations and the experimental results. Therefore the user can rely on the result of the simulation.

This is a chance for the user of these models to simulate unknown topologies or to extend the known topologies into new operating areas. The additional advantage of this procedure is, that not measureable signals can be simulated easily, the interdependency of different components or parasitics can be discussed. The same holds true for different sets of parameters of the components. This gives an opportunity to understand the topology much better and optimize it by simulation. The result is a reduction of practical experiments, the risk and the cost.

THE DEVELOPMENT AND VERIFICATION OF THE HIGH POWER INVERTER

The key technology of a high power HD-GTO voltage source inverter (100 MVA) is the cost-efficient and robust series connection of GTOs. For this 100 MVA inverter six series connected 4.5 kV/3kA hard driven GTOs are necessary. Especially during the development phase simulation tools are of high importance. In the 100 MVA project the SABER-simulator with the mentioned accurate physical semiconductor models was used for the first time [14]. This tool was on the one hand used for the further optimization and the power upgrading of the existing preprototype inverter module to the requirements of the 100 MVA inverter. On the other hand the circuit simulator was used for the concept definition of the connection of up to 24 high power inverter modules at the same DC-link. Due to the first use of the hard driven GTO special attention was given to the event of preflooded freewheeling or snubber diodes. It could be shown that in the case of the switching of a neighboring inverter a current of up to 35 A could exist in the snubber diodes of the di/dt-snubber. In combination with a hard turn-on of a hard driven GTO a possible device failure could be expected.

This investigations resulted in the adding of one RC-snubber over the diodes of the di/dt-snubber (fig. 5), in the reduction of the turn-on di/dt of the HD-GTO (500 A/s) and in the definition of the optimum DC-link topology.

Furthermore this circuit simulator was used for the following verification tasks

- verification of the electrical and thermal design of non-measureable quantities, like for example the current of the snubber diodes
- check of the influence of device tolerances including passive components.

In fig. 6 an example of a worst case simulation by means of the circuit simulator is presented. This simulation was used to check the maximum allowable DC-link voltage of the high power inverter. As worst conditions the following was assumed:

- max. storage time difference of the GTOs of 400ns
- max. DC-link voltage of 12 kV (+20 %) and
- max. tolerance of the snubber capacitors of ± 5 %.

As can be seen the maximum dynamic GTO voltage is in this simulated worst case condition below the limit of 4500 V. More details will be given in the presentation.

CONCLUSION

This paper discusses various design solutions for power electronic circuits like lossless snubber circuits or resonant topologies. These design solutions are valuable, when the power electronic devices are accepted as existing without a deep and critical consideration of the limiting effects inside the power electronic devices themselves. To achieve a more precise understanding of such power electronic topologies and to find optimization rules even in this stage of research and development CAE tools and physical models for the topology design are necessary.

In the second stage of this paper emerging power electronic devices like the hard driven GTO, the GCT, the IGCT and the Trench–devices or new semiconductor material like SiC are described. These emerging devices and material offer new and very promising options in the future.

In the third stage of this paper the CAE design of a 100 *MVA* voltage source intertie with hard driven GTOs is presented. These CAE tools are under development for GCTs and IGCTs for a wider range of applications. Furthermore these physical CAE tools are used to optimize these new power electronic devices from a circuit design point of view.

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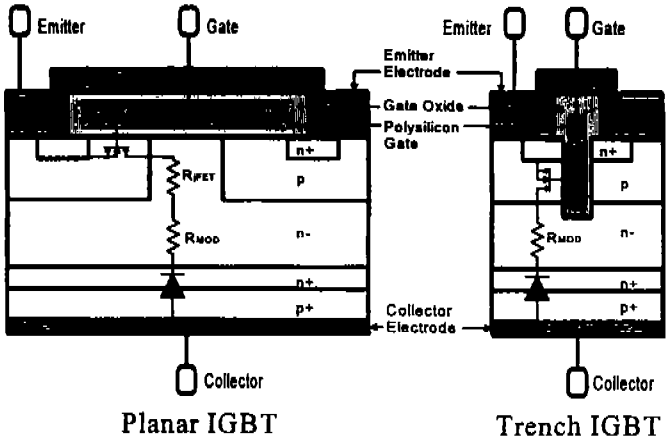

Figure 1: Planar–IGBT and Trench–IGBT

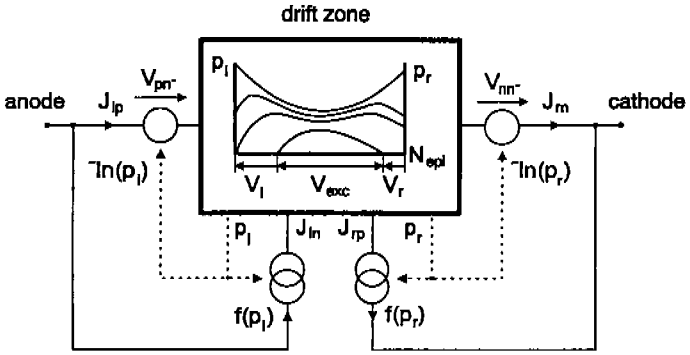

Figure 2: The power diode model

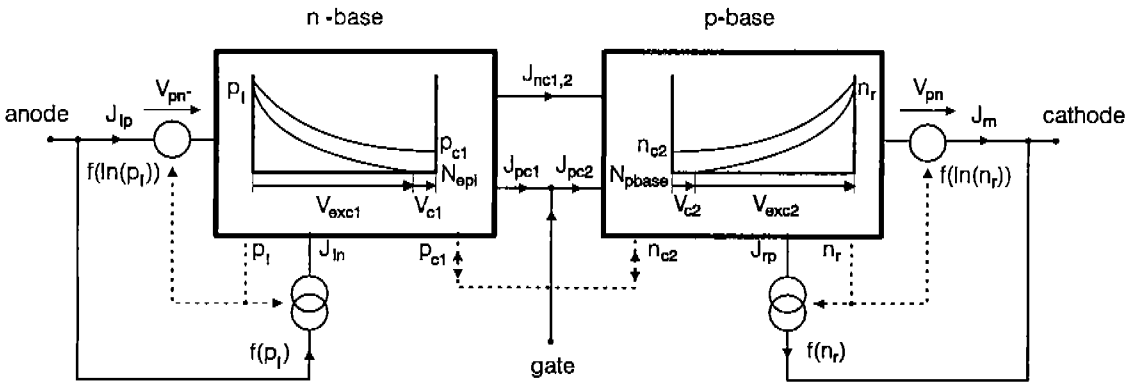

Figure 3: The GTO model

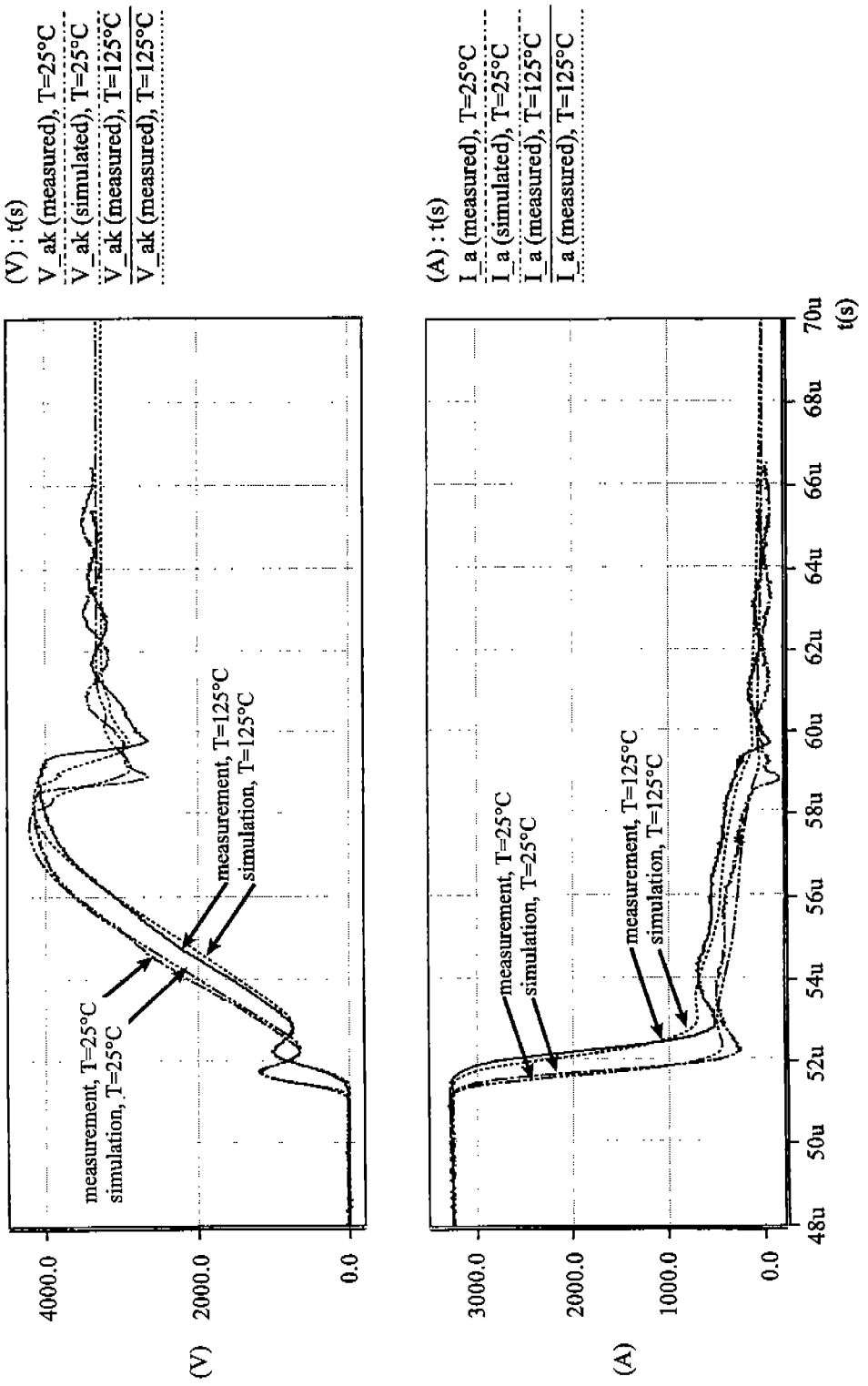

Figure 4: Comparison of the measurement and the simulation of the HD-GTO turn-off at 25 °C and 125 °C

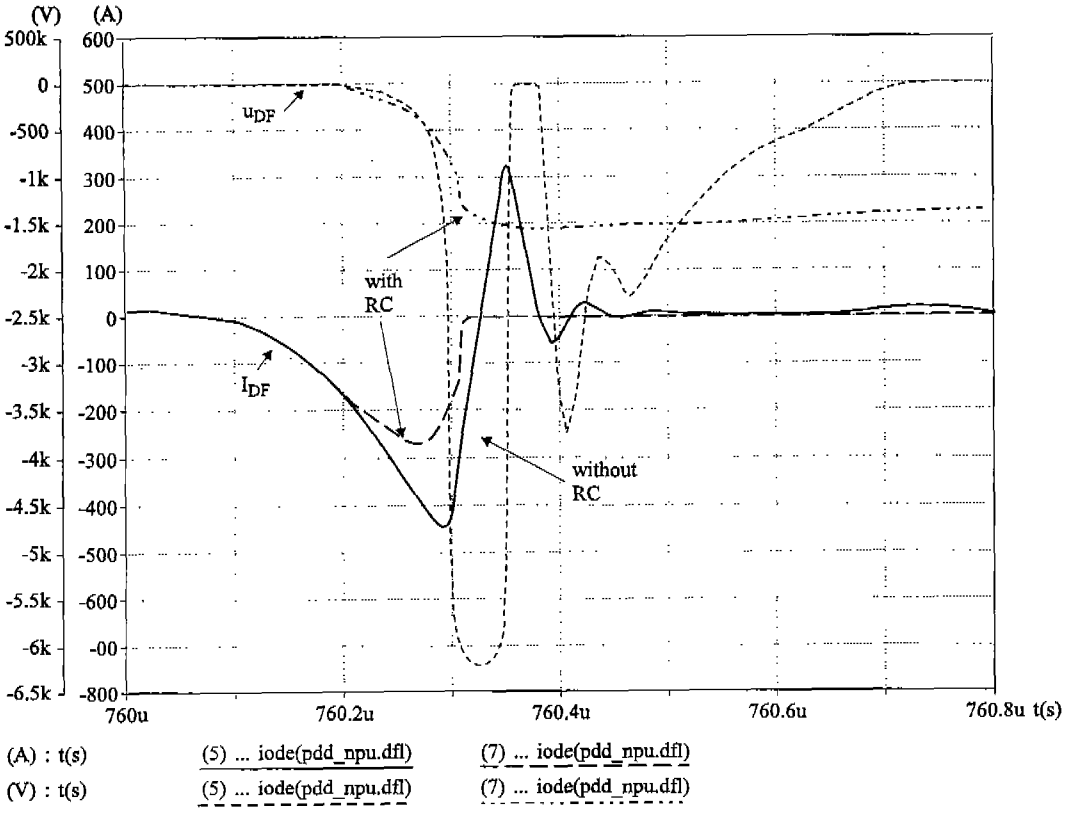

Figure 5: Preflooded snubber diode

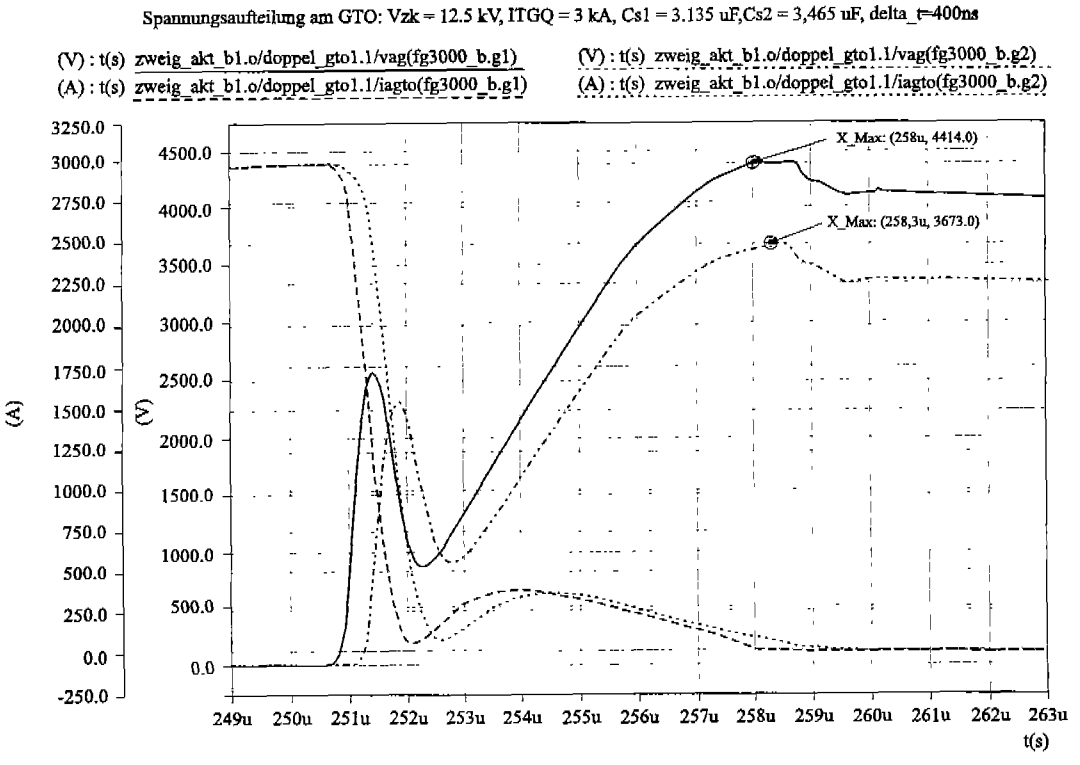

Figure 6: Maximum dynamic GTO voltage in worst case condition