

# A New Parallel Hybrid Filter Configuration Minimizing Active Filter Size

Sukin Park, Jeong-hyoun Sung, and Kwanghee Nam

Department of Electrical Engineering, POSTECH University,  
Hyoja San-31, Pohang, 790-784 Republic of Korea.  
Tel:(82)562-279-2218, Fax:(82)562-279-5699,  
E-mail:kwnam@postech.ac.kr.

**Abstract**—A conventional parallel hybrid active filter has an inherent problem of large current ratings of devices used in inverter. In general, this problem has been solved by adjusting turn ratio of a matching transformer. However, making the transformer with high turn ratio may be not available for high power system due to its requirement for high voltage insulation. In this paper, a new configuration is proposed for parallel hybrid active filter. In the proposed hybrid active filter, the active filter is connected to the passive filter inductor in parallel through a matching transformer for the aim of reducing the size of inverter. Through computer simulations, we have shown the outstanding performances of the proposed topology.

## I. INTRODUCTION

Nonlinear loads, such as diode and thyristor rectifiers and uninterruptible power systems are proliferated in various areas, thus without proper compensation, the quality of power in transmission/distribution systems can be deteriorated. Passive filters are broadly used to reduce the harmonics for their low cost. However, they have some drawbacks: Source impedance strongly affects the compensation characteristics of passive filters. Passive filters are susceptible to undesirable series and parallel resonance with source and loads. Active filters were developed for its flexibility and adaptability to the varying situation. But the use of active filter is limited, due to the limits in semiconductor switch rating and its high construction cost.

Combining the advantages of passive filter and active filter, the hybrid active filter topologies have been developed which enable the use of significantly small rated active filters, compared to pure parallel or series active filter solutions[2]-[5]. In other words, they are cost effective while offering line voltage regulation, and harmonic isolation between supply and load. Another advantage is the easy protection, since possible failures in the active filter do not affect much the load section[7].

There are two topologies for hybrid active filters: One is the series hybrid active filter that consists of the series active filter and the shunt passive filters [3],[9],[10]. In the series hybrid active filter, the active filter is desired to operate as a short-circuit for the line frequency and as an open-circuit for low-order harmonic currents. With this scheme, the harmonics is forced to flow through the passive filters achieving harmonic isolation between source and load. In the parallel hybrid active filter, the active filter provides a low impedance for harmonics so that all the harmonics flow into the passive unit[7]. Such impedance variation techniques have been studied as a harmonic isolation

method by many researchers[2]-[6],[7]-[10]. If the voltage of active filter is controlled to be proportional to its current, it looks like a variable resistor. Fujita *et al.*[4] proposed an idea of suppressing harmonics by increasing the effective source impedance selectively to the harmonic components. Divan *et al.* [5],[6] used the multiple synchronous reference frames(SRF) and low pass filters in extracting the desired harmonic signals and made varying positive or negative inductances with the aim of providing the tuned harmonic sinks.

In this paper, we propose a new topological structure for parallel hybrid active filter which reduces current ratings of the devices used in the inverter. We demonstrate its performance through computer simulations.

## II. SYSTEM CONFIGURATION AND COMPENSATION PRINCIPLE

### A. System Configuration

Fig. 1(a) shows a conventional parallel hybrid active filter in which the active filter is connected to the shunt passive filters through a transformer [4],[5]. The conventional hybrid active filter requires large current ratings of devices in inverter side though their voltage ratings are small. To estimate the device ratings in a inverter, we assume the zero vector state of the inverter as shown in equivalent circuit Fig. 1(b). We can note from Fig. 1(b) that a large fundamental filter current may flow into the inverter side through a transformer with zero vector state. Though the required voltage ratings of the devices used in the inverter are small, the requirement for large current ratings makes the design of the inverter to be inefficient. By selecting properly the turn ratio of the matching transformer, this problem can be overcome. However, making the transformer with high turn ratio may be not available for high power system due to its requirement for high insulation voltage.

Fig. 1(c) shows the proposed circuit configuration, in which the active filter is connected to the filter inductor in parallel through a transformer. The equivalent circuit is shown in Fig. 1(d) with zero vector state. From Fig. 1(d), we can note that the fundamental component of the current flowing through the passive filter capacitor is divided by two parallel connected inductors,  $L_C$  and  $L_{F5}$ . Hence, the fundamental current flowing into the inverter side can be reduced by selecting a proper value of  $L_C$ . Since the fundamental component of the source voltage is almost blocked by the filter capacitor, the required voltage ratings for the

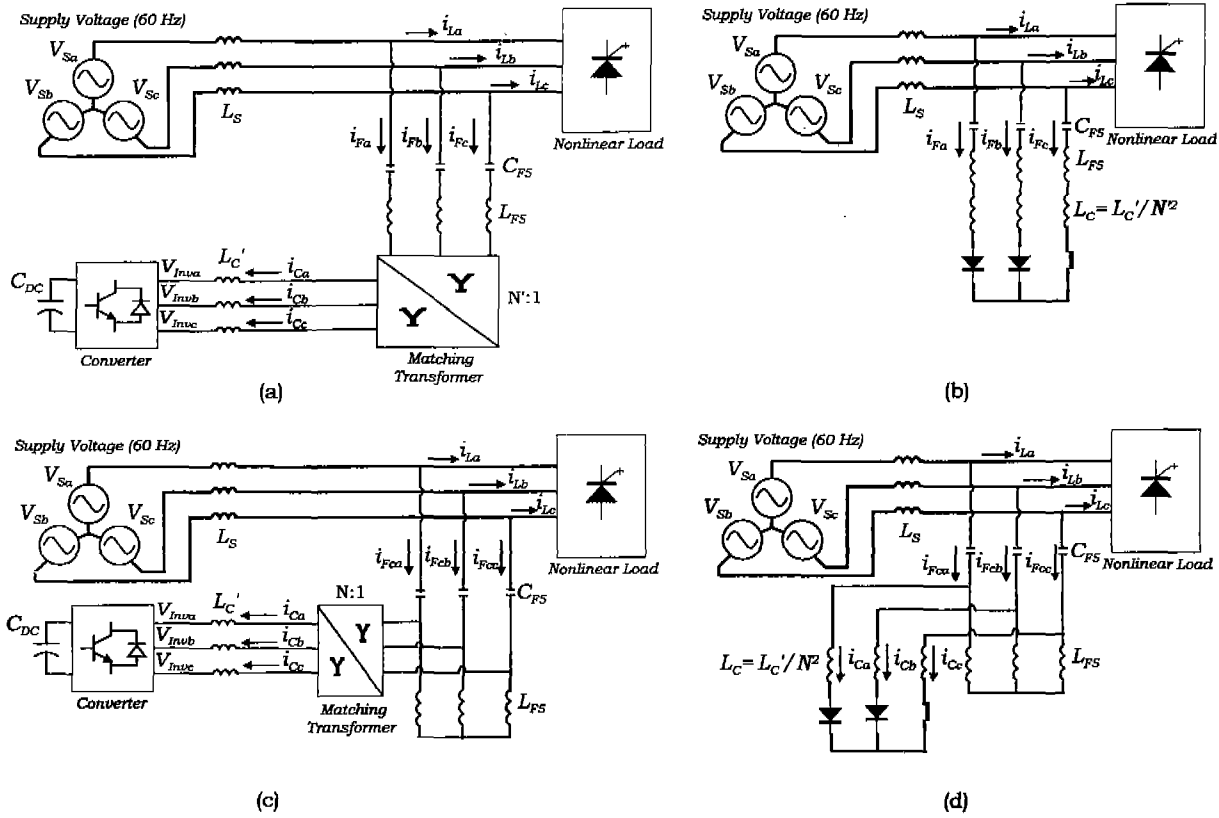


Fig. 1 System configuration (a) Conventional parallel hybrid active filter with 5th passive filter, (b) equivalent circuit for (a), (c) the proposed circuit, (d) equivalent circuit for (c)

ances are almost equal to those of conventional one.

#### Operation principles

Fig. 2(a) shows the equivalent circuit for one phase. Let consider filtering characteristics for the load harmonics and source voltage harmonics. Fig. 2(b) shows the equivalent circuit for harmonics. The system equations in the steady-state concepts are as follows.

$$V_{Sh} = Z_S \cdot I_{Sh} + V_{CFh} + Z_C \cdot I_{Ch} + V_{Inv}, \quad (1)$$

$$V_{Inv} = -Z_C \cdot I_{Ch} + Z_{Fl} \cdot I_{Flh}, \quad (2)$$

$$I_{Sh} = I_{Lh} + I_{Fch}, \quad (3)$$

$$I_{Flh} = I_{Fch} - I_{Ch}. \quad (4)$$

where,  $V_{Sh}$ ,  $V_{CFh}$ , and  $V_{Inv}$  are the source harmonic voltage, the capacitor harmonic voltage of passive filter, and the active filter output voltage, respectively.  $I_{Sh}$ ,  $I_{Lh}$ ,  $I_{Fch}$ ,  $I_{Flh}$  and  $I_{Ch}$  are the source harmonic current, the load harmonic current, the filter capacitor harmonic current, the filter inductor harmonic current, and the active filter harmonic current, respectively,  $Z_S$ ,  $Z_{Fc}$ ,  $Z_{Fl}$  and  $Z_C$  are the source impedance, the capacitors impedance of passive filter, the inductor impedance of passive filter, and the inductor impedance of inverter, respectively.

We assume that the inverter output voltage is controlled to be such that

$$V_{Inv}^* = K \cdot I_{Sh}, \quad (5)$$

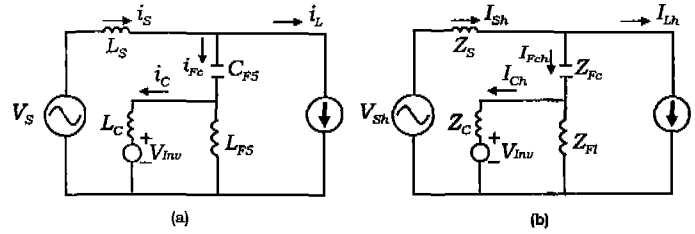


Fig. 2. Equivalent circuit for one phase (a) equivalent circuit (b) equivalent circuit for harmonics

then the source harmonic current  $I_{Sh}$  is given by the following equation:

$$I_{Sh} = \frac{Z_{Fc}}{K + Z_S + Z_{Fc}} \cdot I_{Lh} - \frac{Z_C}{K + Z_S + Z_{Fc}} \cdot I_{Ch} + \frac{1}{K + Z_S + Z_{Fc}} \cdot V_{Sh}. \quad (6)$$

The following ideal filtering characteristics are obtained by assuming that  $K$  is infinite:

$$I_{Sh} = 0, \quad (7)$$

$$V_{Inv} = Z_{Fc} \cdot I_{Lh} - Z_C \cdot I_{Ch} + V_{Sh}. \quad (8)$$

Fig. 3 shows the overall control block diagram for 5th, 7th harmonic elimination. 5th and 7th harmonic components appear as DC quantities in 5th and 7th synchronous

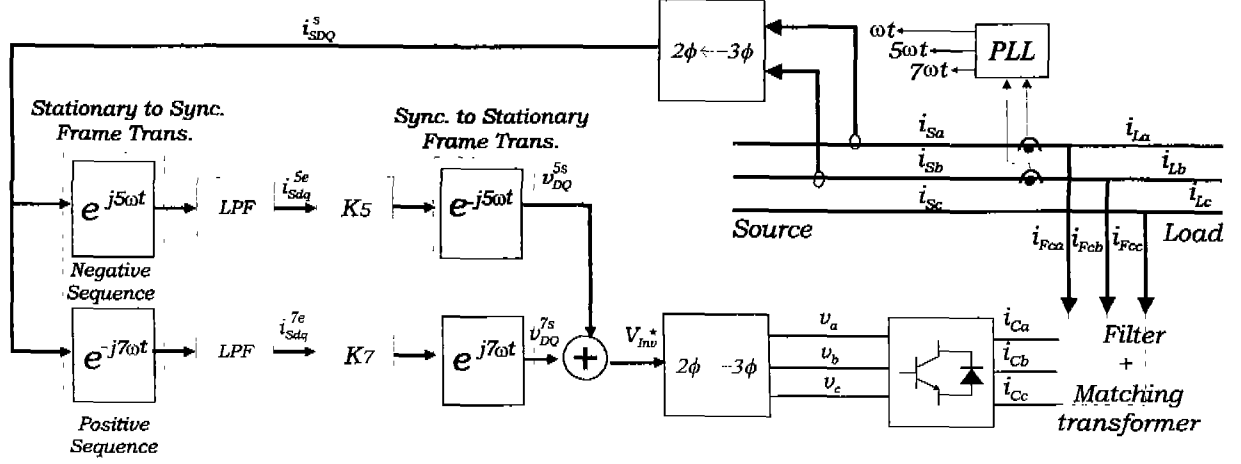


Fig. 3. Control block diagram for 5th- negative sequence and 7th- positive sequence harmonic elimination

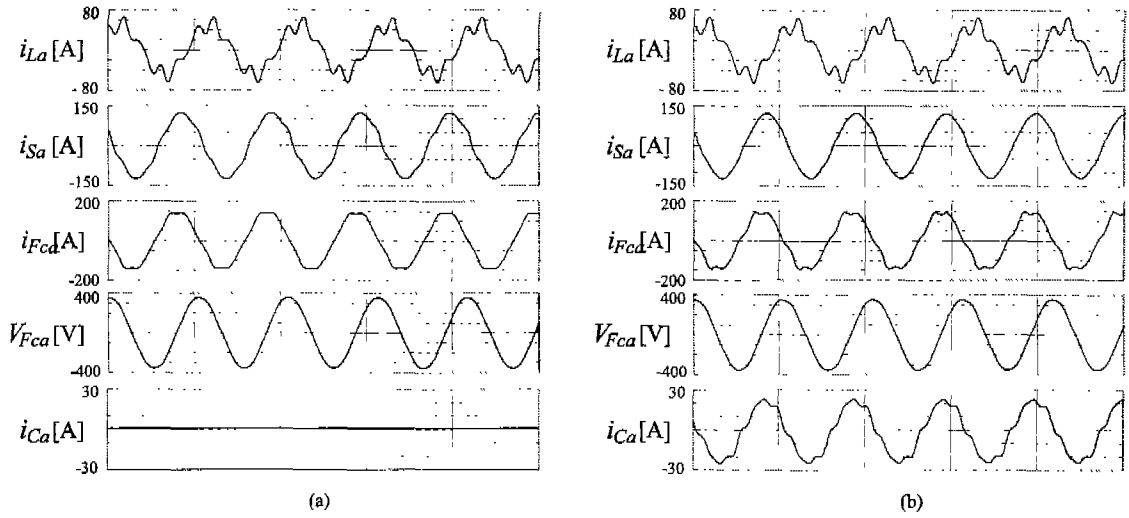


Fig. 4. Simulation results (a) with only passive filters, (b) after 5th and 7th harmonic compensation

reference frames (SRF), respectively. Hence, one can obtain these harmonic components applying low pass filter to the source current in each SRF. Multiplying the measured 5th and 7th harmonic components ( $i_{Sdq}^{5e}$  and  $i_{Sdq}^{7e}$ ) by the constant gain  $K_5$  and  $K_7$ , respectively, and then transforming the results into abc reference frame, we can obtain the inverter control command as shown in Fig. 3.

### III. SIMULATION RESULTS

TABLE I  
THE PARAMETERS OF THE SIMULATION MODEL

$V_S$	$C_{f5}$	$L_{f5}$	$L_C$
440V <sub>LL</sub>	1100μF	297μH	1mH

Performances of the proposed scheme are demonstrated by computer simulations. Table I shows the simulation parameters. Note that the 5th passive filter is mistuned at 4.6th. For the simulation, we let  $L_S = 100\mu H$ , and assume

that the load current is 45° lagging:

$$\begin{aligned}
 i_{La} &= 50 \cos(\omega t - \frac{\pi}{4}) + 12.5 \cos(5\omega t - \frac{5}{4}\pi) \\
 &\quad + 5 \cos(7\omega t - \frac{7}{4}\pi) \\
 i_{Lb} &= 50 \cos(\omega t - \frac{11}{12}\pi) + 12.5 \cos(5\omega t - \frac{55}{12}\pi) \\
 &\quad + 5 \cos(7\omega t - \frac{77}{12}\pi) \\
 i_{Lc} &= 50 \cos(\omega t + \frac{5}{12}\pi) + 12.5 \cos(5\omega t + \frac{25}{12}\pi) \\
 &\quad + 5 \cos(7\omega t + \frac{35}{12}\pi).
 \end{aligned}$$

Note that the 5th harmonic component has negative sequence whereas the 7th harmonic component has positive sequence. One can see that load currents contain 25% 5th harmonic current and 10% 7th harmonic current.

Fig. 4 shows the simulation results. Fig. 4(a) show the results with only passive filters. One can see some distortions in source current due to load harmonic currents.

Fig. 4(b) show the results after the harmonic elimination scheme is applied with the proposed circuit. One can notice from the second plot of Fig. 4(b) that the source current  $i_{Sa}$  becomes remarkably clean. We can note from Fig. 4(b) that the inverter current ( $i_{Ca}$ ) is about 20% of the filter current ( $i_{Fca}$ ). The inverter current ratings are reduced.

#### IV. CONCLUDING REMARKS

We construct a new hybrid active power filter by connecting the inverter output to the inductors of the passive filter in parallel with the aim of reducing the size of inverter. With the proposed configuration, the fundamental component of the current flowing through the passive filter capacitor is divided by the parallel paths of two inductors locating at inverter side and passive filter side, respectively. Hence, the current rating of the inverter can be reduced. Additionally, a harmonic elimination method is suggested for the proposed active filter. This configuration provides the fundamental leading current and the harmonic current paths when the inverter is not in operation. Since the major components of the current pass through the passive filter, the inverter current rating can be reduced.

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