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Fabrication of Micro-Electron Arrays with Tip Conditioning Electrode using Self-aligned Method

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The nanosize Si-tip cathode arrays have been fabricated using reduced mask-pattern techniques. The Si (100) substrate was oxidized as an etch mask layer and the initial etch mask of 2 micron size diameter was patterned with conventional photo-lithography technique. The layer with 300 nm silicon oxide and a photoresist layer was patterned. The 2 micron-diameter silicon dioxide mask patterns were reduced to 1 micron diameter. With careful etching techniques, it could be reduced possibly down to submicron size. The Si post will be fabricated using wet KOH anisotropic orientation dependent technique followed by sharpening oxidation. The reactive ion etching using SF_6 gas was followed in order to have one micron height silicon cylinder. The followed self-aligned gate fabrication techniques were performed. We will fabricate the gate electrode contact in order to have fabricated tip conditioning effect prior to measure the Fowler-Nordheim curve and I-V characteristics[1,2].

References:

1. P.R. Schwoebel, I. Brodie, J. Vac. Sci. Technol., Vol 13, No.4, p1392, (1995)
2. "The Operational Characteristics of Practical HV Gaps," Chapter 2 in *'High Voltage Vacuum Insulation"* edited by R.V. Latham, published by Academic Press Inc. San Diego, CA 92101, 1995