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B-TUE-06

DEPENDENCE OF SUBSTRATE DEFLECTION ON SPACER DISTANCE IN FLAT PANEL DISPLAYS, Y. R. CHO, H. S. KIM, J. Y. OH, and H. S. JEONG(Electronic Materials Lab. - Institute for Advanced Engineering, Yongin P.O. BOX 25, Kyonggi-Do, 449-020, Korea)

The main function of spacer in the flat panel display is to sustain the predetermined spacing between the base and face plates. The objective of this study is to calculate and estimate the change of deflection and stress of substrate dependence on spacer distance in the vacuum sealed panel. The deflection and stress of the substrate were calculated by finite element method using ANSYS software. For calculation of them we assumed that the spacer is a rigid body of 200 μm diameter. The spacer distance varied from 2.5 mm to 40 mm in the vacuum sealed panel, which is composed of 1.1 mm thick soda lime glass. To confirm the calculated results from simulation, we made the panel correspond to the simulation and measured the substrate deflection. The values from the simulation and measure were very similar. When the spacer distance is shorter than 5 mm, the substrate deflection is below 1 μm which is acceptable in the flat panel display.

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B-TUE-07

PREPARATION AND CHARACTERIZATION OF Zn-Ga-o PHOSPHOR THIN FILMS FOR FIELD EMISSION DISPLAY, H. Isogai, Y. Yoshida, and H. Yamamoto (College of Sci. & Tech., Nihon University, 7-24-1 Narashinodai, Funabashi-shi, Chiba, Japan)

A low resistivity, no release of pollution gas, a high efficient emission light, and a stabilization of the surface are needed for phosphors for Field Emission Display (FED). In this work a feasibility of a thin film was paid attention to in order to satisfy the above-mentioned conditions. A Zn-Ga-O thin film was prepared by rf reactive sputtering to develop low voltage electron beam excited phosphor thin films for FED with a high efficient emission blue light and a long life. A $ZnGa_{2-x}O_y$ target used was a sintered disk. The substrates used were ITO, single crystal MgO and $SrTiO_3$. Using a new type of a vacuum system which enables an in-situ characterization of phosphorescent properties without exposing to the air after a film preparation, the films were studies systematically for a phosphorous property by changing the preparation conditions: the composition of the Zn-Ga-O target, a gas pressure, and a substrate temperature. As a one of results obtained an emission of greenish blue light was observed in films which were deposited on about 500 substrates from a ZnGa 204 target.

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B-TUE-08

APPLICATION AND EVALUATION OF Zr-V-Fe+Ti NON-EVAPORABLE GETTER FOR FIELD EMISSION DISPLAYS.

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Though the high vacuum more than ~10^{-6} Torr in an FED is critical to its performance and lifetime, its vacuum level is no more than ~10^{-5} Torr, because of the conductance limitation in the narrow panel gap(200~500 ㎛) and the generated gases during the tip-off process. In this study, we applied the Zr-V-Fe+Ti non-evaporable getter in both the evacuation tube and the panel. The generated gases detected by RGA during the tip-off were H_2, CO, CO_2 and CH_4. Since the getter adsorbed these gases, the vacuum level in the panel was kept 1.6×10^{-5} Torr, which was the same value as that before the tip-off. After this process, the degree of vacuum was improved to 5.5×10^{-6} Torr by the getter activation within the panel. It is concluded that the high vacuum more than ~10^{-6} Torr in the panel with the narrow gap such as a few hundred ㎛ will be achieved by the application of the non-evaporable getter.

B-TUE-09

A Novel Structure of Polysilicon Emitter Arrays with Pedestal Type Resistor for Field Emission Display, JIN HO LEE, YOON-HO SONG, SEUNG-YOUL KANG, KYOUNG IK CHO, SANG YUN LEE* and BO-WOO KIM (Semiconductor Technology Div. ETRI, Taejon, 305-600, Korea, *Dept. of Physics, Kyungpook National University, Taegu, 702-701, Korea)

The gated polysilicon field emitter tip arrays with resistors have been fabricated and characterized. The pedestal type resistors of amorphous silicon were formed by chemical mechanical polishing (CMP) before the formation of emitter tips. The emitter layer was deposited with polysilicon and sharpened by a dry etching process, and the gate aperture was formed by CMP process. Our structure has a merit of the good controllability of the load resistance by changing the height and diameter of the resistor. Also, the pedestal type resistor built-in each emitter tip acts as a current limiter and enhances the life time of emitters. Furthermore, We could form a very small gate aperture even though with a thick gate dielectric using a double layered structure, resulting in the enhancement of electric field at the emitter tip without increasing gate leakage current. All processes were done below 600 ℃, so that the technology could be applied to a glass-based field emission display.