

## Sym. D : Display Materials

### TFT TECHNOLOGIES

#### B-WED-05

INDUCTIVELY COUPLED PLASMA (ICP) OXIDATION FOR LOW-TEMPERATURE POLY-Si THIN FILM TRANSISTORS.

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In low-temperature poly-Si thin film transistors (poly-Si TFTs), high quality poly-Si film and clean oxide/poly-Si interface are the key factors to obtain high performance. Thermal oxidation is a suitable method for preparing gate oxide with clean oxide/poly-Si interface, but growth rate is very low at low temperature. Using an ICP oxidation method, we fabricated gate oxide with clean oxide/poly-Si interface at low temperature (<450°C).

ICP is a high density plasma like ECR plasma and can be enlarged easily. Plasma density was  $3 \times 10^{11}/\text{cm}^3$  at 2 kW, 5 mtorr and increased as the RF power increased and/or the oxygen pressure decreased. The electron temperature was within 3-5 eV. The oxide thickness was grown to 270 Å at 450°C for 60 min in 5 mtorr. The optical emission spectra showed that the oxide thickness was proportional to the intensity of atomic oxygen peak and linear to the oxidation time below 90 min. The growth activation energy by ICP oxidation was 0.19 eV, which was much smaller than that of thermal oxidation. The field effect mobility of TFT with (ICP + LPCVD) gate oxide was 30  $\text{cm}^2/\text{Vs}$ , which was 1.5 times higher than that of TFT with LPCVD gate oxide only.

#### B-WED-06

EFFECT OF DEPOSITION CONDITIONS AT THE HETEROGENEOUS NUCLEATION SITES ON THE CRYSTALLIZATION BEHAVIOR OF LPCVD a-Si FILMS ON SiO<sub>2</sub>, M.-K. RYU, S.-M. HWANG, S.-H. MIN, AND K.-B. KIM (School of Mater. Sci. & Eng., Seoul National Univ., Seoul, 151-742, KOREA)

The microstructures of crystalline phases nucleated at the a-Si/SiO<sub>2</sub> interface and film surface have been comparatively studied during the solid phase crystallization (SPC) of a-Si films deposited on SiO<sub>2</sub>. At a given deposition temperature ( $T_d < 550^\circ\text{C}$ ), it was found that elliptical grains were nucleated at the interface while equiaxed ones nucleated at the surface. However, the interface-nucleation kinetics was much faster than that of the surface-nucleation one. Although the surface nucleation rate could be enhanced by increasing the  $T_d$ (surface), elliptical grains were nucleated from the surface when the  $T_d$ (surface) was increased up to the transition temperature  $T_r$  (~575 °C). Thus, it is important that the  $T_d$ (interface) must be lower than  $T_d$ (surface) and at the same time, the  $T_d$ (surface) should not be higher than the  $T_r$ , in order to obtain a high quality of SPC poly-Si with large equiaxed grains.

#### B-WED-07

METAL-INDUCED LATERAL CRYSTALLIZATION OF AMORPHOUS SILICON FILMS ON GLASS USING RAPID THERMAL ANNEALING,

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There has been continuous research efforts in thin film transistors to grow high quality polycrystalline silicon under the following requirements: (1) at a low temperature, (2) on a large glass substrate, and (3) with a high yield. It was shown that a few nano-meters of nickel-metal film which is deposited on the amorphous silicon film could lower the crystallization temperature, to less than 500°C, and high performance poly-Si TFTs were fabricated with furnace annealing by metal-induced lateral crystallization (MILC). In this research, polycrystalline silicon TFTs could be fabricated by RTA with a tungsten-halogen lamp. RTA-MILC TFTs show higher electron mobility than that of Furnace-MILC TFTs. The differences in electrical properties can be attributed to the different thermal profiles, which can induce differences in micro-structure and concentrations of defects.

## Sym. A : Silicon Process

METALIZATION & INTERCONNECTION- I  
C-WED-01

THE EFFECT OF GRAIN STRUCTURE ON THE CURRENT-DENSITY IN THE BLACK EQUATION FOR AL-BASED INTERCONNECTS, J. H. HAN and M. C. Shin (Div. of Metals, KIST, Cheongryang, Seoul, 136-791, Korea), S. H. Kang (Center for Advanced Materials, Lawrence Berkeley National Laboratory, and Dept. of Materials Science and Mineral Engineering, Univ. of California, Berkeley, CA 94720)

The reliability of Al-based interconnects against electromigration failures has traditionally been predicted by a well-known empirical equation (Black equation). The current-density exponent (n) contained in the Black equation has commonly been known as 2. However, prior work has suggested that the n-value often deviates from 2 significantly, depending on line width and/or applied current-density range. The work reported here focuses on the n-value over a wide range of grain structures in Al-based interconnects. In the case of polygranular structure, the n-value is 1.9, which coincides with the commonly reported number 2. In contrast, the lines that have a mixed structure of small and large grains and a near-bamboo structure show the n value of 2.4 and 3.1, respectively. In keeping with the microstructural mechanisms of electromigration failures, the results of this work further emphasize that understanding grain structures of the interconnects is critical.