Sym. A : Silicon Process

METALIZATION & INTERCONNECTION-Ⅲ

A-THU-09

OPTIMIZATION OF TUNGSTEN PLUG CHEMICAL MECHANICAL POLISHING USING THE DIFFERENT CONSUMABLES, Sung Pyo Jung, Hyo Sang Kim, Sang Yong Kim, Jae Sung Choi, (FAB division, ANAM SEMICONDUCTOR INC. 222, Dodang-dong, Wonmi-gu, Buchon, Kyunggi-Do, KOREA)

The comparison of W plug CMP characteristics using the different slurry of component and pad of hardness have been carried out. Two kinds of slurry were used, and two kinds of pad were used. The polishing has been carried out on an orbital polisher, subsequently PVA brush has been used for cleaning.

The tungsten pattern wafer were prepared by deposition of W(4500Å)/TiN(1200Å)/Ti(380Å) stacks on the 1㎛BPSG that plug holes were formed. After polishing of tungsten plug, surface roughness of oxide film was measured by Atomic Force Microscope(AFM). Results show that the roughness of silica based slurry and soft pad is smaller than that of alumina based slurry and hard pad. The recess and key-hole of W plug according to polishing time were measured by AFM. Results show that recess of peroxide oxidizer slurry is greater than that of potassium iodate oxidizer slurry, and according to over-polishing peroxide oxidizer slurry has make more expanded than potassium iodate oxidizer slurry key-hole in tungsten plug. Oxide erosion which was generated by over-polishing was measured about pattern density and consumable sets respectively. The results show that the erosion is related to hardness of pad and polishing selectivity. After polishing and cleaning using the NH4OH and DIW, Alumina residue was inspected on polished wafer by the alumina based slurry. Also metal contamination in plug was analyzed.

THURSDAY

A-THU-10

THE CHARACTERIZATION OF SHALLOW TRENCH ISOLATION CHEMICAL MECHANICAL PLANARIZATION (STI CMP) THROUGH THE ANALYSIS FOR RELATIONSHIP OF BETWEEN PATTERN AND NON-PATTERN WAFER, YONG-SIK KIM, YANG-WON LEE, DAE-YOUNG KIM, SANG-YONG KIM, JAE-SUNG CHOI(FAB Division, ANAM Semiconductor, 222, Dodang-dong, Wonmi-gu, Buchon, Kyunggi-do, 420-130, KOREA)

Now, most of the end point of oxide CMP have obtained by polishing time calculated from using removal rate and thickness target of oxide. This report is about controlling oxide removal amount on pattern wafer as using removal rate and removal thickness of non-pattern wafer. IPEC 472 polisher was used in this test. Of course, it was polished by optimized process condition. Post CMP cleaning used Standard Chemical(SC-1, NH4OH:H2O2:H2O) and HF chemical. The variation of Shallow Trench Isolation thickness(measured by NANO thickness measurement), Step Height between moat and field region (measured by Profilometer) and STI vertical structure(measured by vertical CD SEM) of specific pattern wafer as polishing time were analyzed. Under the same condition, the blanket wafer was polished and its thickness variation was analyzed as polishing time. While blanket wafer had linear change by polishing time, pattern wafer did not. We found that there is a relationship between the oxide removal amount of blanket(non-pattern) and that of pattern wafer. We analyzed for this relationship, and the post CMP thickness of pattern wafer could be controlled by removal rate and removal thickness target of blanket wafer. And finally in this paper, the result of repeatability test will be showed

A-THU-11

DIRECT INTEGRATION OF PLATINUM ON POLY-SI SUBSTRATES BY METALORGANIC CHEMICAL VAPOR DEPOSITION, EUN-SUCK CHOI and SOON-GIL YOON (Dept. of Materials Engineering, Chungnam National University, Daeduk Science Town, 305-764, Taejon. Korea

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Platinum bottom electrodes are directly integrated on poly-Si/SiO_2/Si(100) substrates by metalorganic chemical vapor deposition (MOCVD) and dc magnetron sputtering. Platinum films deposited directly on poly-Si by MOCVD at 400°C do not form platinum silicide after annealing at 700°C in oxygen ambient. On the other hand, Pt films deposited on poly-Si at 350°C by dc sputtering were changed to form platinum silicide at 700°C. Pt films deposited on poly-Si by MOCVD prevent effectively the diffusion of oxygen and silicon at high temperatures in oxygen ambient. Direct integration of platinum on poly-Si by MOCVD are potentially attractive for nonvolatile and dynamic random access memory application.

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ETCHING & DEFECTS IN Si

A-THU-12

AUTOMIC-LAYER DEPOSITION OF SILICON NITRIDE, SHIN YOKOYAMA, YOSHIMITU NAKASHIMA and KENJI OOBA (Res. Ctr. for NANODEVICES and Systems, Hiroshima Univ., Higashi-Hiroshima 739-8527, Japan)

The target of this study is to fabricate quantum structures such as quantum wires by using selective atomic-layer deposition (ALD) of silicon nitride and silicon on the different materials. The ALD of silicon nitride has been in vestigated by means of (1) plasma ALD in which NH3 plasma is used, (2)thermal catalytic ALD in which NH3 is dissociated by thermal catalytic reaction on W filament, and (3) programed temperature ALD in which only thermal reaction on the substrate is employed. The NH3 and the silicon source gases(SiH2Cl2 or SiCl4) were alternately supplied. For all these methods, the film thic kness per cycle was saturated at a certain value for the wide range of deposition conditions. In the thermal catalytic ALD, the selective deposition of silicon nitride on a hydrogen-terminated Si was achieved, however, it is limited only for thin(<4㎚) film. In the plasma ALD, the selective deposition was difficult due to the hydrogen atoms generated with the NH3 plasma. In the programed temperature ALD, the selective deposition on Si and no deposition on SiO2 succeeded at any growth cycles due to the high-temperature reaction, adsorbed Si+SiO2->2SiO(evaporated), on the SiO2 surface.