Sym. G : Electro-packaging

ADVANCED PACKAGES- I

E-THU-03

ELECTRICAL EVALUATION OF INTERCONNECTS FOR HIGH SPEED MCM APPLIACTIONS, Y.M. LEE, H.O. Park, C.W. Ju, S.B. Lee, J.T. Baek, B.W. Kim (Micro Systems, Semiconductor Tech. Division, ETRI, Taejon, 305-350, Korea)

The electrical characteristics of interconnects for high speed MCM applications are becoming increasingly more important since the clock frequency of devices and the number of simultaneous switching outputs increase. The objective of this paper illustrates the useful design guides of MCM interconnect lines including geometry, dimensions and process parameters. For this work, the practical criteria were used as follows. 1) Attenuation < -2 dB, 2) Return Loss < -20 dB, 3) Crosstalk < -20 dB, 4) Delay Time < 0.2 t_r(signal rising time). It could be seen that the design guides must be considered on the clock frequency and the fabrication ability. Therefore, the analysis was performed in the frequency range up to 2 GHz and two types of substrates such as MCM-L (BT-resin/Cu) and MCM-D (BCB/Cu) were evaluated in this work. A variety of test structures formed by microstrip were prepared. The electrical characteristics of interconnect lines such as characteristic impedance, insertion and return losses, crosstalk, and delay time were evaluated using the network analyzer and time-domain reflectometry. Also, the effects of discontinuities such as via, wire bonding, and bent line were analysed. In addition, the important process parameters in MCM-D were explained.

E-THU-04

A ROBUST AND LOW COST STACK CHIPS PACKAGE, M.K. PARK, D.H. KIM and S.J. CHO (Package Research Dept., Semiconductor Research Div., Hyundai Electronics Industries Co., Ltd., Ichon-si, Kyoungki-do, Korea 467-701)

Stack packaging technology has been studied as one of the solutions providing high density large memory system for PC and Workstation server application by many IC makers. Hyundai Electronics developed its own stack chips package for the stack market. The major characteristics of the package is as follows ;(1) stacking multiple leadframes, (2)joining them using solder or conductive epoxy, and (3) encapsulating them in one package. From the preliminary feasibility test, the technology is expected to be one of most reliable and cost competitive stack packaging solutions. In this paper, the main features of the new stack chips package are briefly introduced in terms of the structure, materials, and processes. The reliability is also discussed.

E-THU-05

NOVEL 3-DEMINSIONAL MEMORY STACK PACKAGES USING POLYMER INSULATED SIDE-WALL, H. S. Ko, J. S. KIM, H. G. YOON, S. Y. Jang, S. D. CHO, and K. W. PAIK, Deptartmemt of Materials Science & Engineering, KAIST, Taejon 305-701, Korea

A novel design of three dimensional (3-D) stacked bare die package has been established. And the prototype of the 3-D package using mechanical dies has been demonstrated. The whole processes of fabricating the 3-D package consist of wafer cutting into die segments, die passivation including sidewall insulation of dies, via opening on I/O pads of die, I/O redistribution from center pads to sidewall, bare dies stacking using polymer adhesives, sidewall metallization and interconnection, and solder balls attachment.
There are several remarkable improvements in this 3-D package design compared with the conventional Irvine Sensors®' and Cubic Memory®'s 3-D packages. The unique features of this newly developed package design are the sidewall insulation prior to the I/O redistribution, which produces 1) better chip-to-wafer yield and 2) significant process simplification in the following fabrication steps. According to this design, 100% dies on a conventional wafer can be used without any neighboring die loss which is due to I/O redistribution. Processes can be simplified during I/O redistribution, sidewall insulation, sidewall interconnection, and package formation. The mechanical integrity of the prototype 3-D stacked package meets the JEDEC Level III and 85C/85% test.

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CSP & BGA PACKAGES

E-THU-06

Bumping, CSPs and Substrates; The new Packaging Materials and Technologies, Shinichi Wakabayashi (R&D Division, Shinko electric Industries Co. Ltd.)

Recently, IC and system packaging technologies have moved to higher density and smaller form factor technologies to achieve higher performance devices at a resonable cost. This technology trend advances change in package types materials, assembly technologies and substrates. This paper covers wafer/chip bumping technologies using thin film and plating technologies, CSP manufacturing processes and reliability such as micro-BGA and SCSP, and tapes and new buildup substrates for CSPs and DCA/Flip Chip assembly The reliability of the buildup substrates will be also discussed.

THURSDAY