Czochralski 법으로 제조된 실리콘 단결정 내의 Flow Pattern Defect와 Large Pit의 열적 거동 및 소자 수율에의 영향

Thermal Behavior of Flow Pattern Defect and Large Pit in Czochralski Silicon Crystals and Their Effects on Device Yield.

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Abstract

Thermal behavior of Flow Pattern Defect (FPD) and Large Pit (LP) in Czochralski Silicon crystals was investigated by applying high temperature (≥1100℃) annealing and non-agitation Secco etching. For evaluation of the effect of LP upon device performance / yield, DRAM and ASIC devices were fabricated. The results indicate that high temperature annealing generates LPs whereas it decreases FPD density drastically, and LP does not have detrimental effects on the performance / yield of device whose design rule is larger than 0.35 ㎛.

Key Words : Czochralski Silicon Crystal, Flow Pattern Defect, Large Pit, Device Yield

1. Introduction

Since Yamagishi et al.[1] reported that Flow Pattern Defects (FPDs) revealed by non-agitation Secco etching in Czochralski (Cz) Silicon (Si) crystals have a detrimental effect on gate oxide integrity, several researchers investigated the nature of FPD and proposed that FPD is associated with interstitial type dislocation loops[2], vacancy-related defects[3], or voids[4].

It is generally accepted that FPD density can be reduced by heat-treating Cz Si wafers at relatively high temperature, and by performing crystal growth with slow crystal growth rate[5]. However, Sadamitsu et al.[6] proposed that even though slow Cz crystal growth rate (~ 0.4 ㎜/min) can be effective to reduce FPD density drastically it generates large pits (LPs) that are large dislocation loops with a diameter about 10 - 30 ㎛. In addition, Takeno et al.[7] suggested that octahedral voids (observed inside the OISF-ring of crystals grown with fast crystal growth rate, 1.4 ㎜/min) and interstitial type dislocation loops (generated outside the OISF-ring in very slowly grown crystals with ~ 0.4 ㎜/min) are revealed either as FPDs or Secco etch pits (SEPs) by non-agitation Secco etching for 30 min., and since they loose their chemical properties it is difficult to find flow patterns after high temperature heat treatment in dry O_2 ambient while the defects themselves remain stable.

In this study, to investigate the nature of LP in Cz Si crystal and its effect on device performance / yield, we evaluated the changes in morphology and radial density profile of FPD and LP in fast-pulled (0.7 ㎜/min) and slow-pulled (0.4 ㎜/min) crystals through various thermal cycles, and DRAM (design rule : 0.38 ㎛) and ASIC (design rule : 0.50 ㎛) devices were fabricated.

2. Experimental

Prime Si wafers of p-type (boron-doped, 6 - 7 Ω·㎝) (100) 200 ㎜ diameter were taken from the middle position of two Cz crystals grown with a medium oxygen crystal growth program by applying different crystal pull rates (0.4 ㎜/min

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and 0.7 ㎜/min). Oxygen and carbon concentrations measured using FTIR system were 12.7 ~ 13.4 ppma and < 0.05 ppma (in new ASTM), respectively. Four kinds of thermal cycles, such as (1) 1100℃, 2 hours, dry oxidation, (2) 1200℃, 2 hours, dry oxidation, (3) 1200℃, 1 hour, wet oxidation, and (4) simulated 4-step based on 16Mbit DRAM process, were used to investigate thermal behavior of FPD and LP. For examination of the changes in radial profiles and morphologies of FPD and LP, non-agitation Secco etching for 30 min (in this case the etched thickness of Si wafer was about 20 ㎛) was applied to as-received and heat-treated samples. Then, the defect density and morphology were investigated using optical microscope. By comparing radial profile of LP with EDS yield map, we tried to figure out the effect of LP upon device yield / performance. In case of device processed wafers, HF solution was used to remove the device layer.

3. Results and Discussion

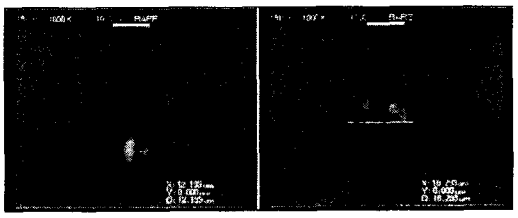
3.1 Thermal Behavior of FPD and LP

FPDs were known as one of the typical vacancy-related grown-in defects which can degrade gate oxide integrity.[1] LPs were reported as an interstitial-related defect that can be observed outside FPD rich area or in the crystals grown with slow crystal pull rate.[6] However, their thermal behavior and effects on device yield / performance are not clarified yet.

Fig. 1 shows micrographs of LPs in the crystal grown with 0.4 ㎜/min. LPs in the crystal grown with 0.4 ㎜/min were composed of either singular or plural shapes and with or without flow pattern. The size of LP was 10 ~ 30 ㎛ while that of the tip of FPD was smaller than 1 ㎛.

The radial distribution of FPD and LP in the crystals grown with 0.7 ㎜/min and 0.4 ㎜/min were shown in Fig. 2. It is clear that FPD level lower than 30 ea/cm^2 can be obtained by performing crystal growth with the slow pull rate of 0.4 ㎜/min, which is in good agreement with the results of previous study.[1,5,6] However, as indicated by Sadamitsu et al.[6] this slow crystal growth generated LPs whereas the crystal grown with the pull speed of 0.7 ㎜/min showed no LP and higher FPD density. In case of the crystal grown with the pull speed of 0.7 ㎜/min, it should be pointed out that there was a boundary at the distance of 70 ㎜ from wafer center where FPD density decreased quickly, which is known as an oxidation induced stacking fault (OISF)-ring. It is said that this OISF-ring divides wafer area into two regions - vacancy- rich region (inside OISF-ring) and interstitial-rich region (outside OISF-ring).[7]

In order to investigate thermal behavior of FPD and LP, adjacent wafers from each crystal were annealed with four kinds of thermal cycles and then inspected under optical microscope after non-agitation Secco etching for 30 min. Fig.3 shows the dependence of FPD and LP densities on heat treatment condition in case of the crystal with the pull speed of 0.7 ㎜/min. These data clearly indicate that FPD can be annihilated by high temperature (≥1100℃) annealing, and the higher the heat treatment temperature, the faster the reduction rate of FPD density. These results



(a) (b)

Fig.1. Optical micrographs of LPs : (a) singular shape without flow pattern and (b) plural shape with flow pattern in as-received wafer (crystal pull speed : 0.4 ㎜/min)

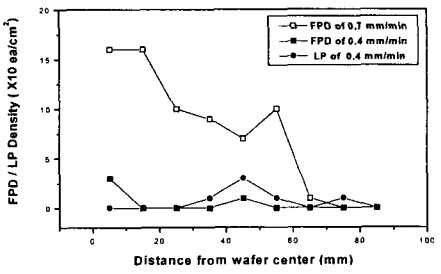


Fig.2. Radial distribution of FPD and LP in as-received wafer (LP was not found in the crystal with the pull speed of 0.7 ㎜/min)

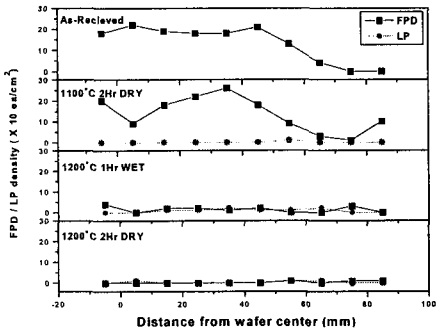


Fig.3. Dependence of FPD and LP densities on heat treatment condition (in the crystal grown with the pull speed of 0.7 ㎜/min)

are in general agreement with those of comparatively extended works on the characteristic of FPD.[4,5]

And, note that LP was generated during high temperature annealing. Its density was lower than 10 ea/cm^2 and almost constant regardless of heat treatment conditions. It is also remarkable that LP generation was not confined within a specific region such as inside or outside OISF-ring in wafer. Judging from these results, it seems that the origins of FPD and LP are fully different.

The data in Fig. 4 reconfirms whether LP generation is confined to a specific region in wafer or not. The samples taken from the crystal prepared with the pull speed of 0.7 ㎜/min were thermally annealed using simulated 4-step based on 16Mbit DRAM process. For verification of the OISF-ring, X-ray Lang topograph was taken with MoKα_1/(440) diffraction after simulated 4-

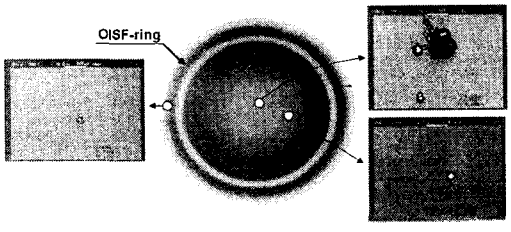
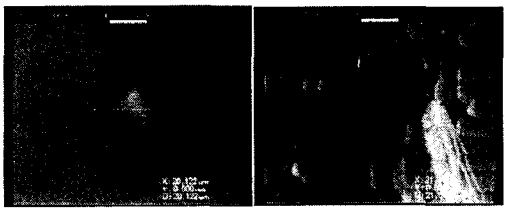


Fig.4. Optical micrographs of LPs and X-ray Lang topograph with MoKα_1/(440) diffraction in the wafer grown with the pull speed of 0.7 ㎜/min (after simulated 4-step based on 16Mbit DRAM process)



(a) (b)

Fig.5. Optical micrographs of LPs (a) without and (b) with flow pattern in ASIC device-processed wafer (crystal pull speed : 0.7 ㎜/min)

step. As observed in Fig. 4, LPs were generated both at the inside and at the outside of OISF-ring through simulated 4-step based on 16Mbit DRAM process. The results from Figs. 3 and 4 are in contrast to the case for the model proposed by Sadamitsu et al.[6], which indicated that LP is generated only at the outside of OISF-ring.

3.2 Effect of LP on Device Yield

In order to investigate the effect of LP on device yield, ASIC (design rule : 0.5 ㎛) and DRAM (design rule : 0.38 ㎛) devices were fabricated and electrical function test was performed.

Fig. 5 shows the shapes of LPs observed in the samples with the pull speed of 0.7 ㎜/min after ASIC device processing. These shapes are just the same as those in the as-received wafers grown with the pull speed of 0.4 ㎜/min as shown in Fig. 1. Therefore, it can be clearly said that LPs were generated in the wafers grown with the pull speed of 0.7 ㎜/min through ASIC device

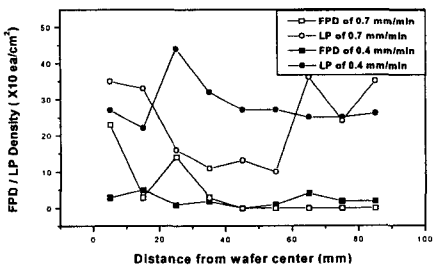


Fig.6. Radial distribution of FPD and LP in ASIC device-processed wafers

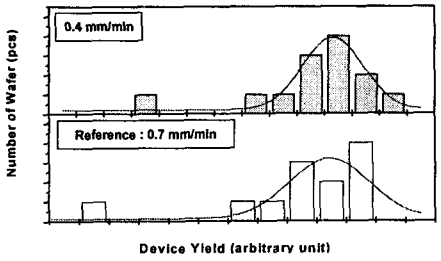


Fig. 7. Device yield comparison between crystals grown with the pull speed of 0.4 ㎜/min and 0.7 ㎜/min after ASIC device (design rule : 0.5 ㎛) fabrication.

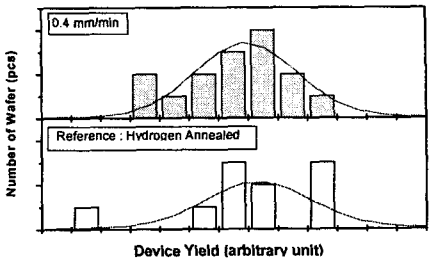


Fig. 8. Device yield comparison between hydrogen-annealed wafer and the crystal grown with the pull speed of 0.4 ㎜/min after DRAM device (design rule: 0.38 ㎛) fabrication.

processing and the average density is about 240 ea/cm^2 (Fig. 6). It is also noticeable that the average density of LP in the samples grown with the pull speed of 0.4 ㎜/min was increased from 6 ea/cm^2 (Fig. 2) to 280 ea/cm^2 (Fig. 6) after ASIC device fabrication. Even though ASIC device-processed wafers contain significant number of LPs, the final device yield on these wafers is kept at a satisfactory level in manufacturing line (Fig. 7). In addition, the wafers (grown with the pull speed of 0.4 ㎜/min) which contain LPs in as-received state showed no yield difference compared to hydrogen-annealed wafers after DRAM device fabrication (Fig. 8).

Judging from these results, it seems that LP does not have detrimental effects on the performance / yield of device whose design rule is larger than 0.35 ㎛.

4. Conclusion

The nature of FPD and LP in Cz Si crystals and their effects on device yield / performance were investigated through high temperature (≥ 1100℃) annealing and ASIC / DRAM device fabrication. The results show that

(1) FPD can be annihilated by high temperature annealing and the higher the heat treatment temperature, the faster the reduction rate of FPD density.

(2) The origins of FPD and LP seem to be fully different since LP was generated at the temperature higher than 1100℃ and its generation was not confined within a specific region such as inside or outside OISF-ring in wafer.

(3) LP revealed by non-agitation Secco etching for 30 min does not have detrimental effects on the performance / yield of device whose design rule is larger than 0.35 ㎛.

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