The Development of a Highly Portable and Low Cost SPOT Image Receiving System

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ABSTRACT

This paper covers the development of a highly portable and low cost SPOT image data receiving system. We followed two design approaches. One is the software-based approach by which most of the real-time processing is handled by software. With the complete software-based design, it is simple to add a function for receiving any additional satellite data. Satellite-specific format handlers including error correction, decompression and decryption can easily be accommodated. On the other approach, we used a general hardware platform, IBM-PC and a low cost SCSI RAID (Redundant Array of Independent Disks), and therefore, we can make a low cost system.

1. Background

Nowadays, many companies provide the whole chain of the SPOT image ground station systems which usually consist of a demodulator, a tape recorder, a embedded preprocessing system and MWD(Moving Window Display). The embedded preprocessing system is implemented to handle each satellite image processing. Since this is a hardware-based system and almost all jobs are processed at the embedded preprocessing system the system must be huge and expensive. If plan to receive and archive different satellite image, have to obtain different preprocessing modules. (SPOT,1998) (Datron, 1996) (Shin et al.,1998)

Today, the personal computer technologies have become to meet some of the remote sensing

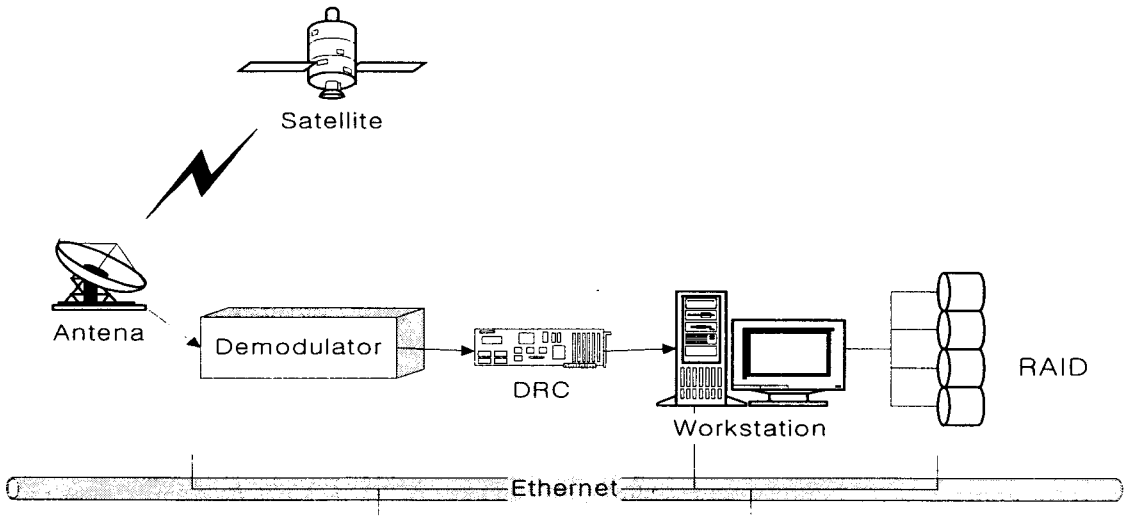

Fig1 Block diagram of system

community's needs. The dramatic improvement in the performance of personal computers including the high speed of CPU clock and low cost main memory, enable to design software-based system. Since the high performance personal computer is generalized, we can construct a high performance platform at low cost.

The hardware technologies required for constructing the SPOT image receiving system are a high bandwidth interface, a high performance computer and high bandwidth storage system. For the high bandwidth interface, apply a high speed signal processing gate logic, a high speed and high density FIFO and high bandwidth parallel interface. The interrupt processing technology and DMA(Direct Memory Access) technology help the high performance I/O processing. We can achieve complex functional logic by using a high bandwidth and high density FPGA(Field-Programmable-Gate-Array) technique. The necessary software technologies are a high bandwidth interface device driver, high-speed display technique and multi-thread handling technique.

2. System Architecture

For developing a highly portable system, the hardware architecture must be so simple. If all satellite-specific functions are implemented by using hardware, different receiving hardware should be implemented for each satellite. The software's flexibility is higher than the hardware's and therefore we can obtain the higher portability at software based system.

The developed system consists of a Direct Receiving Card (DRC), a computer with real-time processing software and a RAID system (see Fig1). The DRC converts the serial ECL (Emitter Coupled Logic) input from a demodulator to parallel data. Since no processing is done in DRC, the downlink data is transferred to the host computer memory and then saved into RAID without any format conversion. The software processes almost necessary jobs; store image data at main memory , de-scramble, de-format, MWD(Moving Window Display), archive at the RAID system.

3. Hardware architecture

We have three hardware design requirements. The first is simple architecture by using commercial hardware. The second requirement is that the system should support the sufficient bandwidth for receiving SPOT image. The third is that this hardware architecture takes the burden of the CPU load of the processing computer.

The hardware technique requirements are a high bandwidth interface, high performance computer and high bandwidth storage system. We used a commercial computer and a storage system, which is the SCSI RAID. We applied the interface techniques to

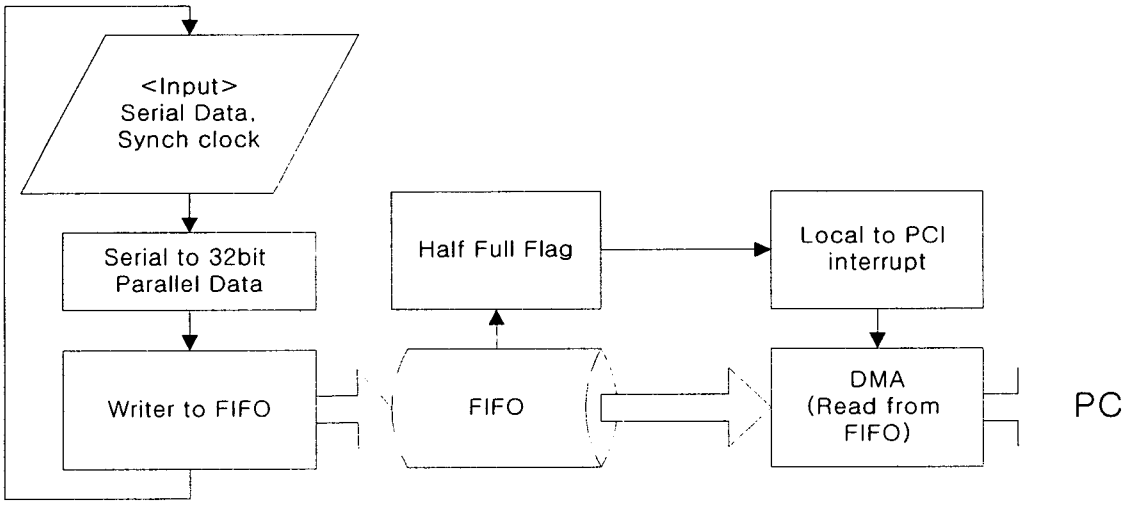

Fig2 Operation Concept of the DRC(Direct Receiving Card)

satisfy the requirements; ECL gates for high speed signal processing, a high bandwidth and high density FIFO and a commercial PCI interface chipset which supports the high bandwidth parallel interface. The PCI chipset supports the interrupt I/O method and the DMA(Direct Memory Access) transfer method. In this section, the major hardware component of the system, DRC, is described.

Fig2 shows the operation concept of the DRC. The serial ECL input data is converted to 32bit parallel data and stored in FIFO, The local interrupt occurs when FIFO half-full flag is set. When the receiving software in PC recognizes the local interrupt, the FIFO data is transferred to main memory of the PC by the bus mastering DMA (Direct Memory Access) technique.

Fig3 shows signal flow between each component in the DRC. The main components of DRC are a receiver component, a FPGA, a FIFO and a PCI chipset. The receiver component receives a stream of ECL data and synchronous clock from the demodulator. FPGA logic generates control signal(1) and control signal(2). The control signal(1) enables the data to be written to FIFO. The control signal(2) enables data to be transferred from FIFO. The PCI chipset has a local interrupt processing function and a DMA(Direct Memory Access) function.

DRC is connected with a demodulator by two coaxial cables, which are a data and a synchronous clock connector. The demodulator outputs are ECL level signal and high frequency, and therefore the receiver component is consisted by using ECL gate logic. Fig4 shows the block diagram of a receiver component. The serial-to-parallel module decreases the frequency of the data. The ECL logic's response time and rise-time are very fast than TTL logic therefore handle the high frequency signal. The ECL-to-TTL module converts the ECL level to TTL level signal.

The FPGA dramatically reduced the

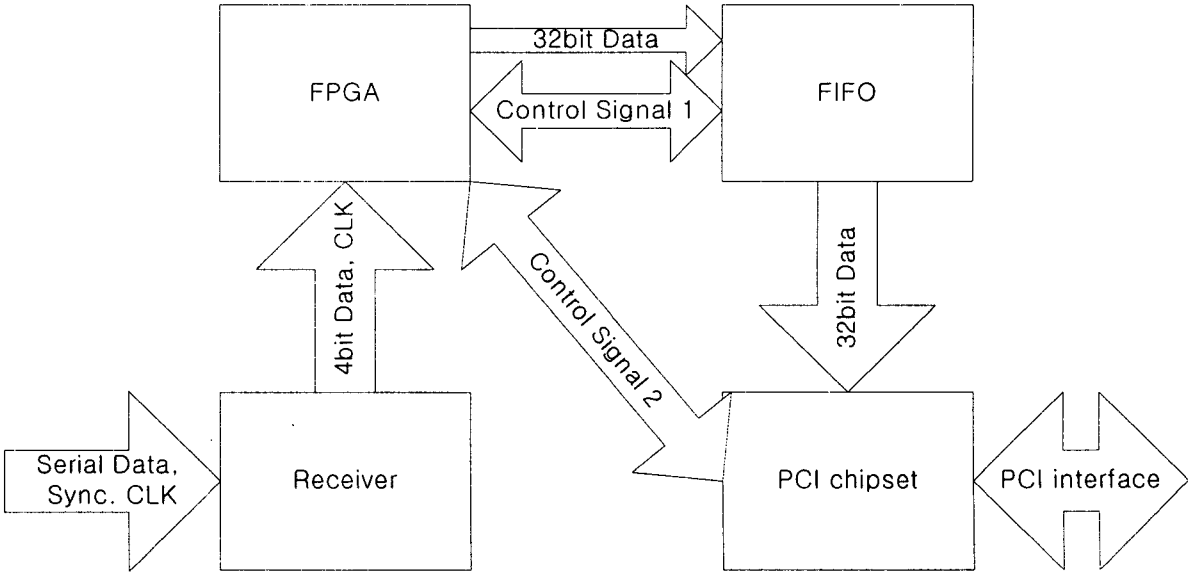

Fig3 Signal flow between each components of DRC

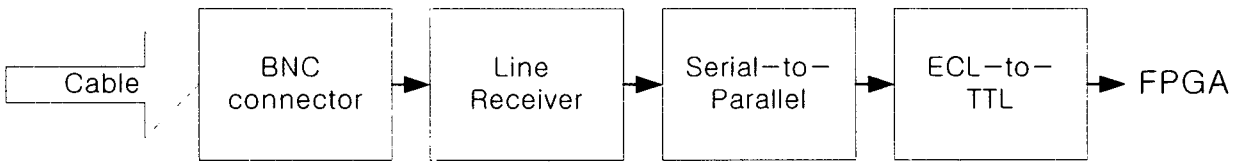

Fig4 Block diagram of receiver component

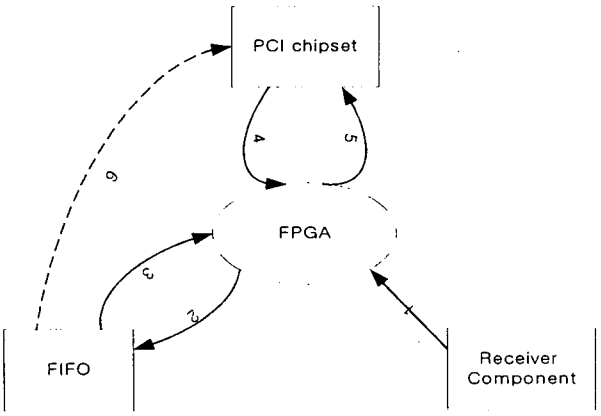

Fig5 The context diagram of FPGA logic

complexity of circuit. The FPGA logic contains almost control signal generation functions. Fig5 shows the context diagram of FPGA logic. It is connected with all modules of the DRC. The FPGA logic' processing sequence divided four steps. First, receives the input data from receiver component, and merges the input data to 32bit parallel data. Second, generates the FIFO writing signal and write the 32bit data to the FIFO. Third, generates the local interrupt signal when the FIFO half-full flag is set. Fourth, generates the read control signal of FIFO using the control signal of PCI interface chipset.

4. Analysis of SPOT 1,2,3 Image Data Encoding

Before image data is downlinked to ground stations, the image data must be combined with various items of data from the satellite bus and formatted into "telemetry frames".(SPOT,1998) Fig6 shows it more specifically. Data compression, data formatting, data scrambling are processed sequentially.

The multi-spectral mode is not compressed and mono-spectral mode is compressed by DPCM compression technique. (SPOT, 1998) The image data are accompanied by ancillary data from the satellite bus. These ancillary data are essential input for ground-based image processing. The ancillary data is composed of 64bit frame synchronization words and 944 bit of ancillary data. Fig7 shows the format of SPOT telemetry frames. All telemetry data except frame synchronization words are scrambled in all transmission modes by "modulo 2" addition with a synchronous-bit-rate pseudo-noise code. The code length is 2047 bits. (SPOT, 1998)

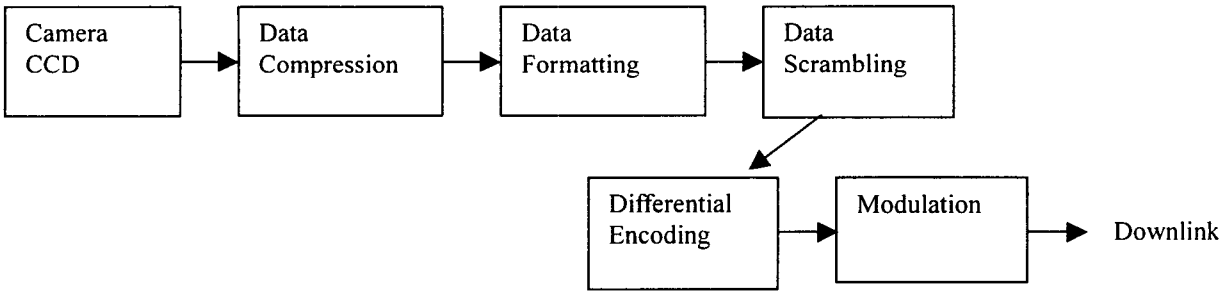

Fig6 SPOT Onboard Image Processing

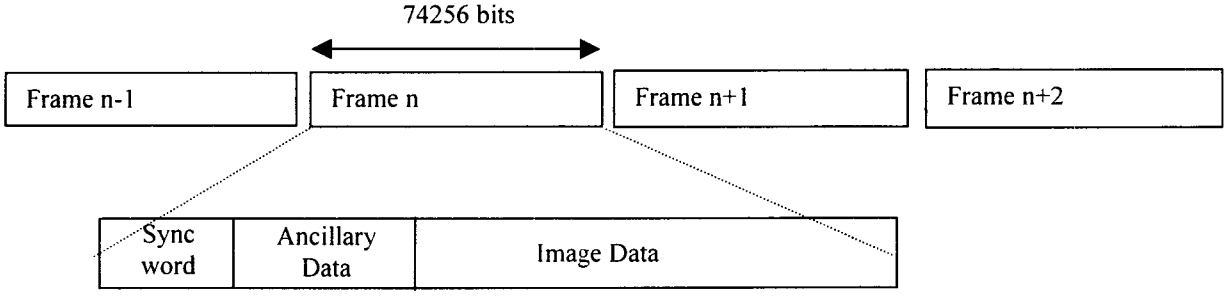

Fig7 The format of SPOT telemetry frames

5. Software Architecture

The software is composed of two threads. One is an I/O handler thread and the other is a de-formatter and moving window display (MWD) thread. The I/O handler thread transfers the input data from DRC FIFO to main memory by using the functions supported by device driver of DRC and saves the input data to RAID in real time. This thread has higher priority than the other thread. The de-formatter thread processes the reverse sequence of SPOT onboard image processing.

Fig8 shows the state diagram of this software. Firstly I/O handler thread is initialized and it waits for a local interrupt. If a local interrupt occurs, it transfers the FIFO data using the DMA transfer function. Then it archives the input data at RAID system. It checks the state of the de-formatter thread. If the de-formatter thread is not running, the I/O handler thread creates a new de-formatter thread for real-time processing and MWD. And the I/O handler thread goes to the wait-state for the next local interrupt.

The I/O handler's processing must faster than the local interrupt frequency. For satisfy this condition, we have to extend FIFO memory size, increase the CPU performance sufficiently and use high bandwidth storage system. We accept the SCSI RAID system for secondary storage system. The highest bandwidth of the ultra SCSI RAID system is 40MB/s, it sufficient our requirement. The advantages of using a RAID storage system are as follows.

- The input data is saved immediately to the RAID in the computer compatible form (file format).
- RAID level 3 provides capabilities for recording data striped across to a number of drives, with error detection codes. This results in high speed and highly reliable data recording.

The downlinked SPOT image is encoded at onboard system. Fig7 shows the sequence of the encoding. We have to process the reverse sequence of

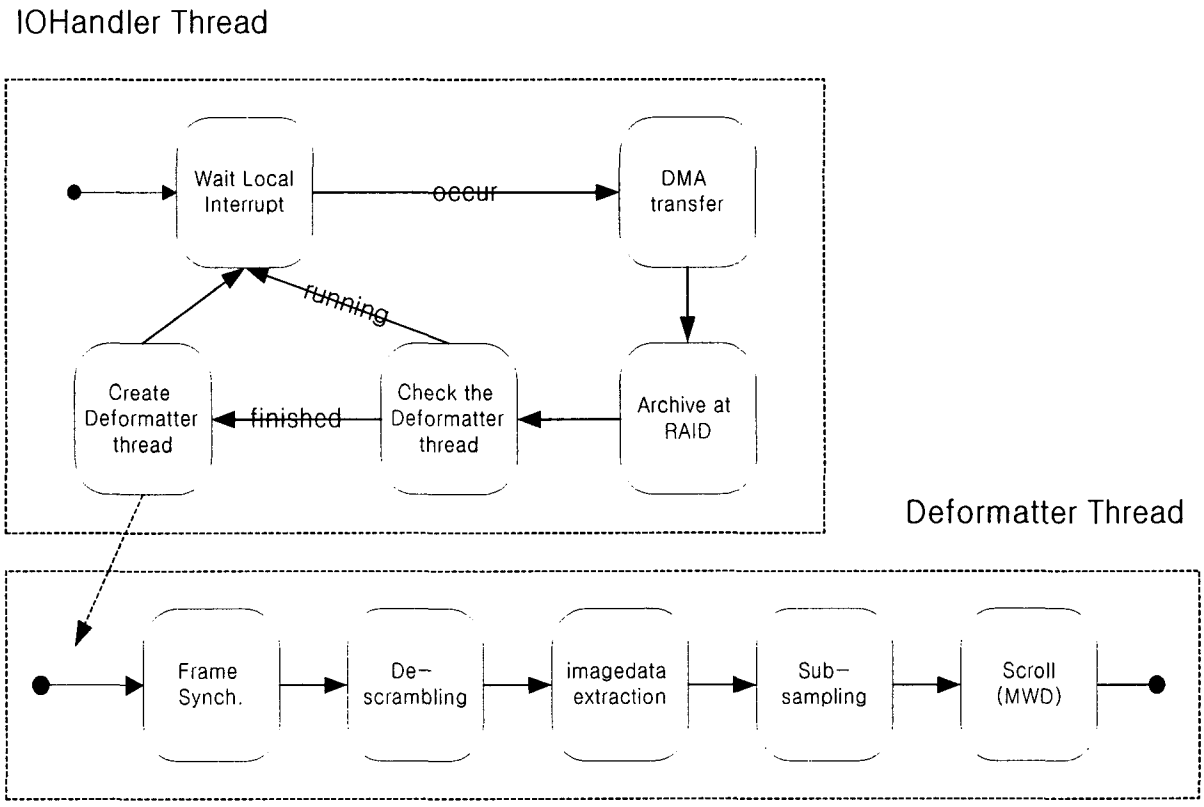

Fig8 The simple state diagram of the I/O handler thread and De-formatter Thread

the SPOT image encoding process for getting the pure image. The de-formatter thread process this sequence processes and the MWD process. Therefor the de-formatter thread functions are divided to decoding for getting the pure data and MWD functions.

For getting pure image data, first detects the frame synchronization words and de-scrambling the frame data except the frame synchronization words. After separates the pure image data from this frame. For MWD, we must sub-sample from the full resolution image because the display monitor's resolution is very low than the SPOT full image resolution. After sub-sampling, display the data using the overlay method.

6. Conclusion

This paper described the highly portable and low cost SPOT image data receiving system. For implement the highly potable system, we minimized the hardware dependency and almost functions were implemented by software. The software developed in modular-based for maximizing the reusability. The low cost computers achieved by using a commercial PC and a low cost SCSI RAID system.

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