High Performance Image Downscaler using Two-Dimensional Phase-Correction Digital Filters†

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이차원 위상-교정 디지털필터를 이용한 고성능 영상 축소기

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요약

본 논문에서는 이차원 위상-교정 디지털필터를 이용한 고화질 디지털 영상축소기에 관한 알고리듬과 하드웨어 구조를 제안한다. 제안된 축소기는 수직방향으로 1/32 line과 수평방향으로 1/64 pixel의 정밀도를 가진 비선형 위상 필터를 사용하여 고화질의 축소 화상을 제공한다. 최적화된 하드웨어 구조를 달성하기 위하여, 디지털필터는 shifter와 adder를 이용하여 구성한다. 마지막으로 시뮬레이션을 통해서 기존의 1/32 scaler[1]의 결과와 비교하여 제안된 방법의 우수성을 보인다.

I. Introduction

Image scaling is widely used in multimedia video applications, such as PC video, camcorder, and so on[2-3]. The geometric transformation of the digital images is inherently a sampling process. As with all sampled data, digital images are susceptible to aliasing artifacts[4]. There are two solutions to remove this aliasing noise: raise the sampling rate or bandlimit the input. The first solution is ideal but may require a bulky hardware that is too costly or sometimes impracticable. The second solution forces the signal to conform to the low sampling rate by attenuating the high frequency components that give rise to the aliasing artifacts.

As with one-dimensional sampled date, digital images experience aliasing artifacts when the input image is downscaled (or undersampled). A simple way to the downscaling is a pixel drop in which the information in every two pixels (or lines) will be dropped. However, it contains the artifacts. [1] showed some improvements by using 2-D digital filters having 1/16-line and 1/32-pixel precisions for vertical and horizontal directions, respectively (hereafter, called 1/32 scaler). The 3dB bandwidth(BW) is about 3.6MHz that is relatively narrow to pass most of video signals of upto 6MHz components. Thereby, an improvement is required somehow to enhance the precision of the scaler while preserving a higher BW and a low hardware complexity.

This paper proposes a high performance image downscaler having 1/32-line and 1/64-pixel precisions for vertical and horizontal scalings

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(hereafter, called 1/64 scaler). The 1/64 scaler is discussed in Section Ⅱ and the characteristics of the vertical and horizontal filters are discussed in Section Ⅲ. The experimental results are described in Section Ⅳ and the conclusions are summarized in Section Ⅴ.

Ⅱ. 1/64 scaler

High frequency components will be folded down in the lower frequency region through a decimation process. Even though antialiasing filter is used to remove the aliasing noise, image degradation is inevitable with the non-integer downscaling[5-7]. For the scaling ratio of 1/2.546875, the required precision of the scaling is 1/64 of a pixel clock since $2.546875 = 1/64 \times 163$. In other words, 64 points should be interpolated between adjacent pixels. In order to achieve the precision, one should use a pixel clock of 64 times faster than that of the original image. In result, the upsampling processor increases the hardware complexity almost proportional to the precision ratio or is sometimes infeasible due to the requirement of a very high speed signal processor.

The proposed 1/64 scaler in this paper uses the concept that valid scaled pixels (or lines) between adjacent pixels (or lines) can be calculated by shifting the group delays of digital filters. Fig. 1 shows the procedure of the scaler using two dimensional phase-correction digital filters. The role of the filters is similar to an all pass filter for gain, while the group delays of digital filters vary according to the scaled points. This can be achieved by changing filter coefficients based on the scaling ratios. Since video signals are generally band-limited in frequency, a low pass filter which passes the bandlimited signals and shifts group delays to the assumed positions is enough to play the role of the two dimensional phase-correction digital filters[1].

Fig. 2 shows the block diagram of the 1/64 scaler. It consists of the following four blocks: (i) line memory, (ii) vertical scaler, (iii) horizontal scaler, and (iv) FIFO memory. The line memory contains two horizontal delay memories. The vertical scaler is comprised of a vertical filter and a vertical discrete time oscillator(DTO). The horizontal scaler is composed of a compensation filter, a horizontal filter, and a horizontal DTO. The FIFO only stores valid downscaled data vertically and horizontally in the right side of the buffer.

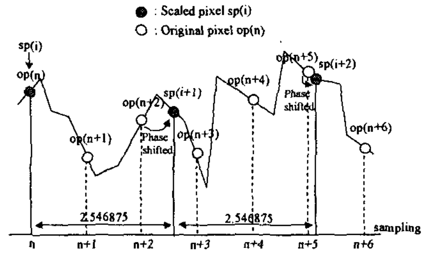


Fig. 1. Proposed high performance downscaler with scaling ratio = 1/2.546875.

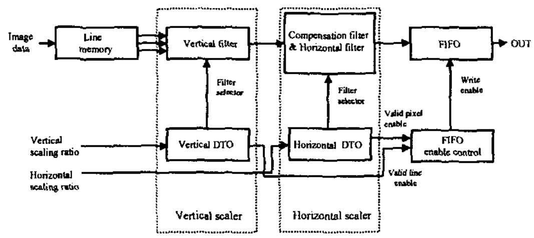


Fig. 2. Block diagram of 1/64 scaler.

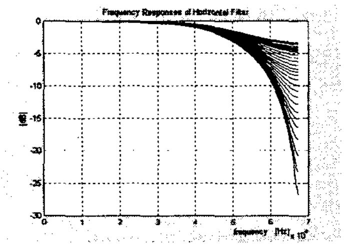
Ⅲ. Characteristics of scaler filters

A 3-tap digital filter having 32-poly phases is chosen for the vertical scaler since one can use incoming, one-line delayed, and two-line delayed data through the line memory. The precision of the scaler is 1/32 line due to the 32 phases in vertical direction.

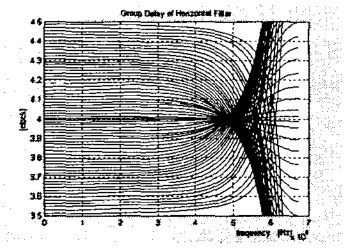
A 5-tap 64-phase digital filter is used for the horizontal scaler. The operating pixel clock is 13.5MHz in frequency to meet the ITU-R BT. 601[8]. The Matlab computes the filter coefficients, and the first-two and last-two filter coefficients out of the 64 are quoted:

$$h_1[n] = -2x[n] + 252x[n-1] + 264x[n-2] - 2x[n-3] + 0x[n-4]$$
$$h_2[n] = -5x[n] + 248x[n-1] + 271x[n-2] - x[n-3] - x[n-4]$$
$$\cdots\cdots \quad (1)$$
$$h_{63}[n] = -x[n] - x[n-1] + 271x[n-2] + 248x[n-3] - 5x[n-4]$$
$$h_{64}[n] = 0x[n] - 2x[n-1] + 264x[n-2] + 252x[n-3] - 2x[n-4]$$

As one can see, all the coefficients can be simply implemented by using shifters and adders since 252 = $2^7+2^6+2^5+2^4+2^3+2^2$. The gain normalization factor of the filter is 1/512. The horizontal filter is cascaded with a compensation filter of a 5-tap FIR type to boost high frequency components up. The characteristics of the filter with the compensation filter are shown in Fig. 3. Fig. 3(a) shows overall frequency responses where the 3dB point is about 6.0MHz in frequency, which is wide enough to pass most of video signals. Fig. 3(b) shows the group delays calculated by the 64 combinations of the filter coefficients. The delays are located within ± 0.5 clock centered at 4 clocks. Thus, the 1/64-pixel horizontal precision is achieved. The 13.5MHz clock is used through entire downscaler. Thereby, the proposed downscaler can be implemented with much less hardware compared with a downscaler using the upsampling.



(a) Frequency responses



(b) Group delays

Fig. 3. Characteristics of the horizontal scaler.

Ⅳ. Experimental results

In order to evaluate the performance of the 1/64 scaler, two input sources are used: (i) 4MHz input signal and (ii) circular zone plate (CZP) image. The 13.5MHz clock is used to quantize the sources and an 1/3 scaling ratio is used to compare the performance of the 1/64 scaler over the 1/32 scaler.

Fig. 4 shows the scaled results obtained by using the 4MHz input signal. The signal is sampled with the 13.5MHz to produce 300 samples. Since the 1/3 ratio is used for the scaling, the size of the scaled signal is now reduced to 100. The dotted line represents the ideally generated-scaled signal. The maximum and minimum amplitudes (hereafter, called max and min) are 126.00 and -126.00, respectively. The dashed line is obtained by using the 1/32 scaler. The max and min are reduced to 77.00 and -77.40 due to the narrow bandwidth and the low scaling precision of the 1/32 scaler. The solid line is obtained by using the 1/64 scaler proposed in this paper. Notice that the values are now increased to 111.69 and -111.66, which shows a great improvement. Another criterion is made for the evaluation. It is the signal-to-noise ratio(SNR) of scaled signals. The SNR is calculated as

$$SNR \equiv 10 \log_{10}\left(\frac{\text{signal power}}{\text{noise power}}\right). \qquad (2)$$

The 1/32 scaler produces the SNR of 78.29 dB. The 1/64 scaler improves the SNR to 80.62 dB, which is very close to the ideal SNR of 80.91 dB. Table 1 summarizes these observations.

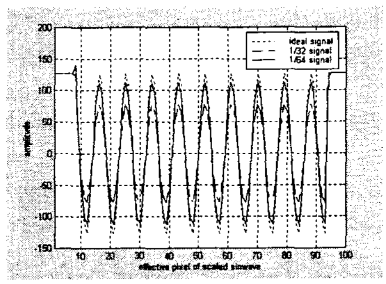


Fig. 4. 1-D plot of scaled signals.

Table 1. Performance evaluation of scalers.

	Ideal	1/32 scaler	1/64 scaler
Max Amp.	126.00	77.00	111.69
Min Amp.	-126.00	-77.40	-111.66
SNR(dB)	**80.91**	78.29	**80.62**

The 2-D CZP image is chosen for another evaluation since it contains the components of 0Hz to 6.75MHz frequencies. Fig. 5 shows the image having 300×300 pixels. The white area around the

CZP image represents blanking periods in horizontal and vertical directions, which will not be shown on the displayed monitors in real applications. Fig 6 shows the scaled images with the 1/3 scaling ratio. The images are now reduced to 100×100 pixels. Fig. 6(a) is obtained by using the 1/32 scaler. Fig. 6(b) is obtained by using the 1/64 scaler. Notice that Fig. 6(b) shows much more components in horizontal direction compared with Fig. 6(a). It is an improvement of the 1/64 scaler since it provides a wider bandwidth and a higher precision over the 1/32 scaler. Once again, one can see the superior performance of the 1/64 scaler.

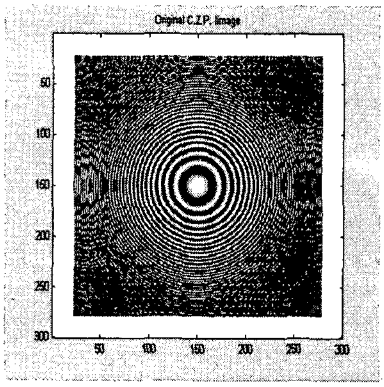
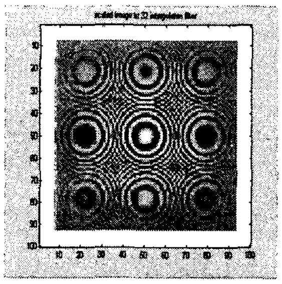
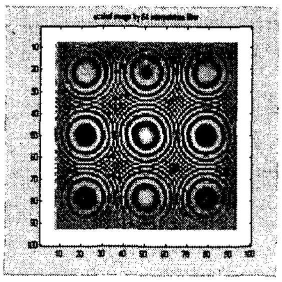


Fig. 5. Original image of CZP having 300×300 pixels.



(a) 1/32 scaled image



(b) 1/64 scaled image

Fig. 6. Scaled CZP images with an 1/3 scaling ratio.

V. Conclusions

This paper proposed an improved performance of the 1/64 scaler. The proposed scaler provided higher precisions of an 1/32 line and an 1/64 pixel in vertical and horizontal directions, compared with the 1/32 scaler. It also provided a wider bandwidth of 6MHz. It was also shown that the scaler could be implemented easily with a low hardware complexity.

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