

# 90-265V<sub>rms</sub> 입력범위를 갖는 단일전력단 역률개선 컨버터

이준영, 구관본, 박희정, 윤명중

한국과학기술원

## A Single-Stage Power Factor Correction Converter for 90-265V<sub>rms</sub> Line Applications

Jun-Young Lee, Kwan-Bon Koo, Hee-Jhung Park, and Myung-Joong Youn

Department of Electrical Engineering  
Korea Advanced Institute of Science and Technology

**Abstract** - A single-stage power factor correction AC/DC converter with a simple link voltage suppressing circuit (LVSC) for the universal line application is proposed. Using this simple circuit, a low link voltage can be realized without deadbands at line zero-crossings. The proposed converter is analyzed and a prototype converter with 5V, 12A output is implemented to verify the performance. The experimental results show that the link voltage stress and efficiency are about 447V and 81%, respectively.

### I. INTRODUCTION

Conventional off-line switching power systems usually include the full-bridge rectifier and large filter capacitor at their input stage. This initial solution produces significant harmonics, which cause the poor power quality and problems to the public utility

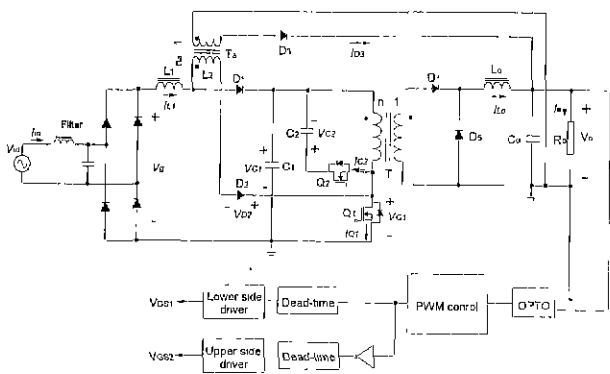


Fig. 1 Proposed AC/DC converter

network. Recently, many nations have release standards such as IEC 61000 and IEEE 519 which impose a limit on the harmonic current drawn by equipments connected to AC line in order to prevent the distortion of an AC line. To cope with these Fig.

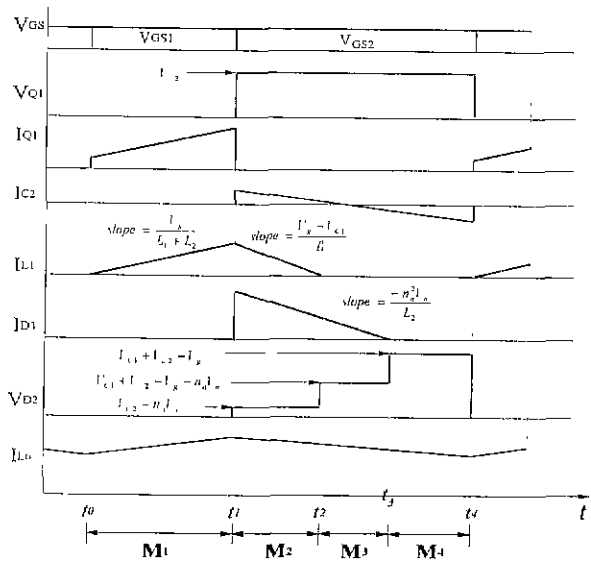


Fig. 2 Key waveforms for mode analysis when  $V_c > n_2 V_o$

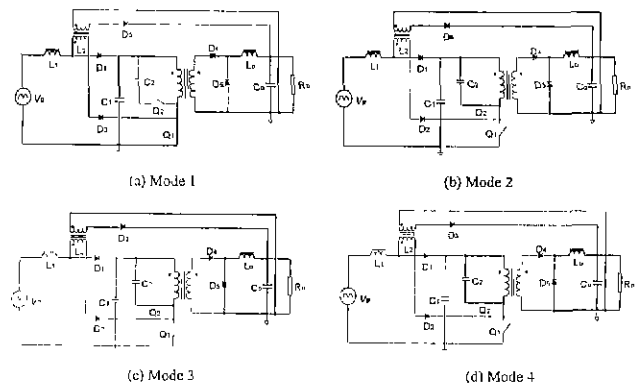


Fig. 3 Topological states of the proposed converter

2 standards, the boost topology operating in a continuous conduction mode(CCM) is the most widely used method. However, this approach is not applicable in low power level applications requiring a low cost and small size. Until now, many

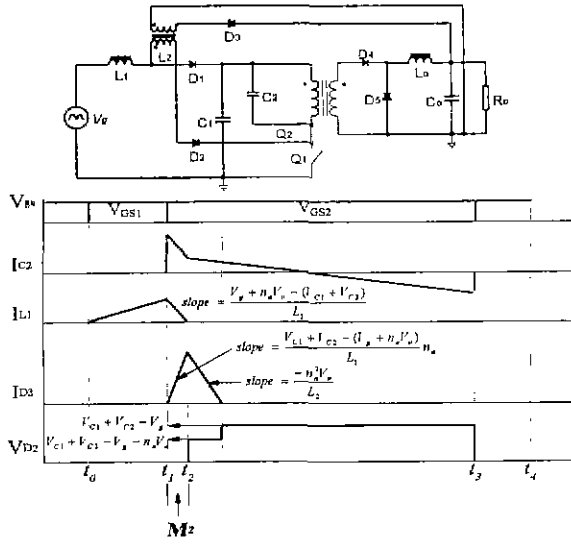


Fig. 4 Key waveforms of mode 2 when  $V_c < n_a V_o$

single-stage topologies have been suggested by combining the PFC stage with a DC/DC converter into one stage[5]. This scheme has a characteristic such as the link voltage should be varied under load changes to maintain an input-to-output balancing. Without developing a new topology or adopting a proper control, the voltage stresses on the link and components such as diodes and switches may be increased. To reduce the link voltage stress, a variable switching control method and a pulse width modulation control method have been suggested, but they have problems such as the low conversion efficiency and/or difficulty of optimal design of filter and inductor[6]. This problem can be solved by S<sup>4</sup>-PFC AC/DC Converter using the magnetic feedback concept[7] and two-switch forward with the auxiliary circuit has been proposed[8]. However, it shows a deadband at line zero-crossings which influences on the harmonics and the link voltage stress stays a higher level than 500V at 265V<sub>rms</sub> line voltage and the auxiliary circuit is somewhat complex.

This paper presents another method derived from basic DC/DC converters and a simple link voltage suppressing circuit(LVSC) to operate on the universal line voltage with a high quality line current waveform, a good efficiency and a low link voltage stress. By transferring some portions of the energy charged in a boost inductor to a load through LVSC, the link voltage stress can be reduced since the link capacitor can hold only a small energy. In this paper, a 60W(5V, 12A output) converter is designed

and tested using the forward topology with active-clamp circuit for transformer reset.

## II. OPERATIONAL PRINCIPLES

Fig. 1 shows the circuit diagram of the proposed converter. The function of a link voltage suppressing circuit(LVSC) consisting of diode  $D_3$  and transformer  $T_a$  is to prevent the boost inductor current  $I_{L1}$  from building up excessively and transfer the energy charging in  $T_a$  to a load without passing by the link capacitor. It can make the boost inductor current flow in a discontinuous conduction mode(DCM) over entire line and load ranges and help to suppress the link voltage stress. The converter operation is analyzed in detail according to four modes as shown in Fig. 2 and their topological states are shown in Fig. 3.

### Mode 1 ( $t_0 \leq t < t_1$ )

This is an on-state interval of the main switch  $Q_1$ . At  $t_0$ , the main switch is turned on and the current flowing through the inductor  $L_1$  and auxiliary transformer  $T_a$  increases as follows:

$$I_{L1} = \frac{V_g}{(L_1 + L_2)}(t - t_0) \quad (1)$$

where  $L_2$  is the primary magnetizing inductance of  $T_a$ . During mode 1, the diode  $D_3$  is blocked and the energy charged in  $C_1$  is transferred to the load via the main transformer  $T$ .

### Mode 2 ( $t_1 \leq t < t_2$ )

Mode 2 begins when  $Q_1$  is turned off at  $t_1$ . The clamp capacitor  $C_2$  absorbs the magnetizing energy of the main power transformer and the voltage stress on  $Q_1$  is clamped by  $V_{C2}$ . As shown in the key waveforms of Figs. 2 and 4, the current path of  $I_{L1}$  may be formed differently according to the voltage condition across  $C_2$ .

#### Case 1 : $V_{C2} \geq n_a V_o$

When  $V_{Q1}$  increases to  $V_{C1}$ , the diode  $D_1$  is forced to conduct and the cathode-to-anode voltage across the diode  $D_2$  is applied as follows:

$$V_{C1} + V_{C2} - n_a V_o - V_{C1} = V_{C2} - n_a V_o. \quad (2)$$

Thus,  $I_{L1}$  circulates through  $L_1$ ,  $C_1$ , and the input source, and is expressed as

$$I_{L1} = I_{L1}(t_1) + \frac{V_g - V_{C1}}{L_1}(t - t_1) \quad (3)$$

where  $I_{L1}(t_1)$  is the initial condition of mode 2. At end of mode 1, the energy charged in the auxiliary transformer during mode 1 starts to be transferred to the load. As can be seen in Fig. 2, the diode current  $I_{D3}$  can be written as

$$I_{D3} = n_a I_{L1}(t_1) - \frac{n_a^2 V_o}{L_2} (t - t_1). \quad (4)$$

### Case 2 : $V_{C2} < n_a V_o$

In this case,  $D_1$  maintains to be off-state since the anode voltage of  $D_1$  stays below the cathode voltage. It makes  $D_2$  be on-state and the current path of  $I_{L1}$  is formed through  $D_2$ ,  $C_2$ ,  $C_1$ ,  $L_1$ , and the input source as can be seen in Fig. 4. In addition, the diode of the auxiliary circuit  $D_3$  is forced to be on-state. Therefore,  $I_{L1}$  decreases linearly with a slope different from case 1 as follows:

$$I_{L1} = I_{L1}(t_1) + \frac{(V_g + n_a V_o - V_{C1} - V_{C2})}{L_1} (t - t_1). \quad (5)$$

Since  $D_3$  is on-state, the reflected current of the boost inductor current  $I_{L1}$  is transferred to the load through  $D_3$ . This current is expressed as

$$I_{D3} = \frac{(V_{C1} + V_{C2} - V_g - n_a V_o) n_a}{L_1} t. \quad (6)$$

Case 2 may be happened at a light load since the control duty becomes narrower as a load becomes lighter, which causes the clamp capacitor voltage  $V_{C2}$  to become lower. Using the volt-second balance condition, the boundary condition between two cases can be found as

$$\frac{DV_{C1}}{1-D} \leq n_a V_o \quad (7)$$

where  $D$  means the control duty of the proposed converter. This equation can be expressed as

$$D \leq \frac{n_a V_o}{V_{C1} + n_a V_o}. \quad (8)$$

### Mode 3 ( $t_2 \leq t < t_3$ )

After the boost inductor current  $I_{L1}$  is reduced to zero, the blocking voltage of  $D_1$  is increased as

$$V_{D1} = V_{C1} + V_{C2} - V_g - n_a V_o \quad (9)$$

and the diode current  $I_{D3}$  decays to zero before the next mode begins. This diode current can be expressed as

$$I_{D3} = I_{D3}(t_2) - \frac{n_a^2 V_o}{L_2} (t - t_2) \quad (10)$$

where  $I_{D3}(t_2)$  is the initial condition of mode 3.

### Mode 4 ( $t_3 \leq t < t_4$ )

Finally,  $I_{C2}$  flows toward the main transformer  $T$  through the clamp capacitor  $C_2$  and the auxiliary switch  $Q_2$  which has been in on-state from the previous mode. When the main switch  $Q_1$  is turned on again, the converter enters mode 1 and the next cycle begins.

## III. ANALYSIS

### A. Expressions of Link voltage

The link voltage expression can be derived from the fact that the charging current to the link capacitor equals to the discharging current from it when the main switch is turned off in the steady state. The charging current is calculated from averaging the current flowing in  $L_1$  during off-state of the main switch over a switching period. This current is given as

#### Case 1 :

$$I_{charge} = \frac{1}{R_e} \frac{L_1 V_g^2}{(L_1 + L_2)(V_{C1} - V_g)} \quad (11)$$

#### Case 2 :

$$I_{charge} = \frac{1}{R_e} \frac{L_1 V_g^2}{(L_1 + L_2)(V_{C1} + V_{C2} - V_g - n_a V_o)} \quad (12)$$

where  $R_e = D^2 T_s / 2(L_1 + L_2)$ , and  $T_s$  means the switching period. The discharging current is the output inductor current reflected to the main transformer primary side when the main switch is turned on and it can be found by subtracting  $I_{D3}$  from the load current since the output power is supplied through LVSC as well as the main power stage. Thus, the discharging current can be expressed as follows:

$$I_{discharge} = \frac{D}{n} \left( \frac{V_o}{R_o} - I_{D3} \right). \quad (13)$$

Thus by averaging over a switching cycle like  $I_{charge}$ , eq. (13) can be rewritten as

#### Case 1 :

$$I_{discharge} = \frac{D}{n} \left( \frac{V_o}{R_o} - \frac{L_2 V_g^2}{R_e V_o (L_1 + L_2)} \right) \quad (14)$$

#### Case 2 :

$$I_{discharge} = \frac{D}{n} \left( \frac{V_o}{R_o} - \frac{L_2 V_g^2}{R_e V_o (L_1 + L_2)} - \frac{L_1 n_a V_g^2}{R_e (L_1 + L_2)(V_{C1} + V_{C2} - V_g - n_a V_o)} \right). \quad (15)$$

As a result, by averaging eqs. (11), (12), (14), and (15) over half a line cycle again, the following equations are obtained.

#### Case 1:

$$V_{C1} = \frac{0.852 n^2 V_{g,rms}^2 + \sqrt{2} K_1 V_{g,rms}}{K_1} \quad (16)$$

where

$$K_1 = \frac{(L_1 + L_2) n R_e V_o^2 D - n^2 V_{g,rms} L_2 R_o D}{L_1 R_o V_o}$$

#### Case 2:

$$V_{C1} = \left( \frac{0.852(n + D n_a)^2 V_{g,rms}^2 + \sqrt{2} K_2 V_{g,rms}}{K_2} + n_a V_o \right) \times (1 - D) \quad (17)$$

where

$$K_2 = \frac{(L_1 + L_2)(n + Dn_a)R_e V_o^2 D - (n + Dn_a)V_{g,rms}^2 L_2 R_o D}{L_1 R_o V_o^2}$$

### B. Selection guideline for turns ratio of $T_a$

The distortion of the line current may be increased if the auxiliary transformer is not completely reset during off-state of the main switch. Thus, the diode current  $I_{D3}$  should be decreased to zero at the worst case before the main switch conducts. Since modes are divided as explained in case 1 at a the worst case, the DCM condition of  $I_{D3}$  can be found from Fig. 2. The duration in time of the diode current  $I_{D3}$  decaying from  $I_{D3}(t_1)$  to zero is

$$t_3 - t_1 = \frac{L_2}{n_a^2 V_o} I_{D3}(t_1) = \frac{L_2}{n_a V_o} I_{L1}(t_1). \quad (18)$$

From eqs. (1) and (17), the DCM of  $I_{D3}$  over the entire line and load changes is guaranteed by

$$\frac{\sqrt{2} V_{g,\min} L_2}{n_a V_o (L_1 + L_2)} D_{\max} T_s \leq (1 - D_{\max}) T_s. \quad (19)$$

Therefore, the turns ratio of the auxiliary transformer should be designed to satisfy the following equation as

$$\frac{\sqrt{2} V_{g,\min} L_2 D_{\max}}{V_o (L_1 + L_2) (1 - D_{\max})} \leq n_a. \quad (20)$$

### C. Derivation of Design Equations

In order for the proposed converter to operate properly, it is important to select appropriately the transformer turns ratios  $n$  and  $n_a$ , the boost inductor  $L_1$ , and the magnetizing inductance of the auxiliary transformer seen from the primary side  $L_2$ . To assure the performance of the converter over the entire line and load conditions, the boost inductor current  $I_{L1}$  should decay to zero at the worst case before the next cycle begins. Since the worst case happens at a minimum line voltage and a full load, the link voltage expressed as in eq. (16) can be used.

Using the relationship between the link voltage and the output voltage, the link voltage expression in eq. (16) can be rewritten as follows:

$$V_{Cl} = \frac{\sqrt{2} V_{g,rms} K_2 V_o^2}{K_2 V_o^2 - 0.852 D^2 V_{g,rms}^2} \quad (21)$$

where

$$K_1 = \frac{(L_1 + L_2) R_e V_o^2 D^2 - V_{g,rms}^2 L_2 R_o D^2}{L_1 R_o V_o^2}$$

The DCM condition of the boost inductor should be considered when the inductor values are selected. The expression of DCM condition of  $I_{L1}$  can be found in a similar way of finding the DCM condition of the diode current  $I_{D3}$  as

Table 1 Key components list

$L_1$	50 $\mu$ H	$D_1, D_2$	D8L60
$L_2$	120 $\mu$ H	$D_3$	S60SC6M
$L_o$	50 $\mu$ H	$D_4, D_5$	DF20LC20U
$C_1$	220 $\mu$ F (440 $\mu$ F/400V in series)	Bridge diode	D6SB60L
$C_2$	1 $\mu$ F	$Q_1, Q_2$	APT8075BVR
$C_o$	3300 $\mu$ F	$n$	8.67(26T:3T)
PWM chip	UC3823N	$n_a$	8(16T:2T)

$$D_2 = \frac{\sqrt{2} V_{g,rms} L_1 D}{(V_{Cl} - \sqrt{2} V_{g,rms})(L_1 + L_2)} \leq 1 - D \quad (22)$$

where  $D_2$  is the ratio of the time needed for  $I_{L1}$  to decay to zero after the main switch is turned off. The values of  $L_1$  and  $L_2$  designed at the worst case with eqs. (21) and (22) guarantee the boost inductor current to flow in DCM.

## IV. EXPERIMENTAL RESULTS

To verify the performance of the proposed converter, a prototype converter with 5V, 12A output is designed and Table 1 is key components list. The measured line current waveforms and link capacitor voltage stresses for 90V<sub>rms</sub>, 120V<sub>rms</sub>, and 265V<sub>rms</sub> line voltage are shown in Fig. 5. The filtered line current follows the line voltage without distortion at line zero-crossings and the link voltage waveform at 265V<sub>rms</sub> line. Fig. 6 shows that the measured power factor is above 0.96 under universal line condition in case that the load is 30% or higher. In addition, Fig 7 is the plot of IEC 61000-3-2 class D limits and measured line current harmonics at  $V_g=120V_{rms}$  and a full load condition. From this figure, the prototype converter meets the harmonic regulation with a sufficient margin. Fig. 8 shows the link capacitor voltage under the line and load variations. The maximum link voltage stress is 447V. Finally, the maximum measured efficiency is about 81%.

## V. CONCLUSIONS

In this paper, a single-phase single-stage AC/DC converter in universal line applications is proposed based on a forward topology with an active clamp circuit and analyzed. Using a simple LVSC, the link voltage stress can be reduced without distortion of the line current at line zero-crossings. From the link voltage expressions, design equations are found and a prototype converter with 5V, 12A

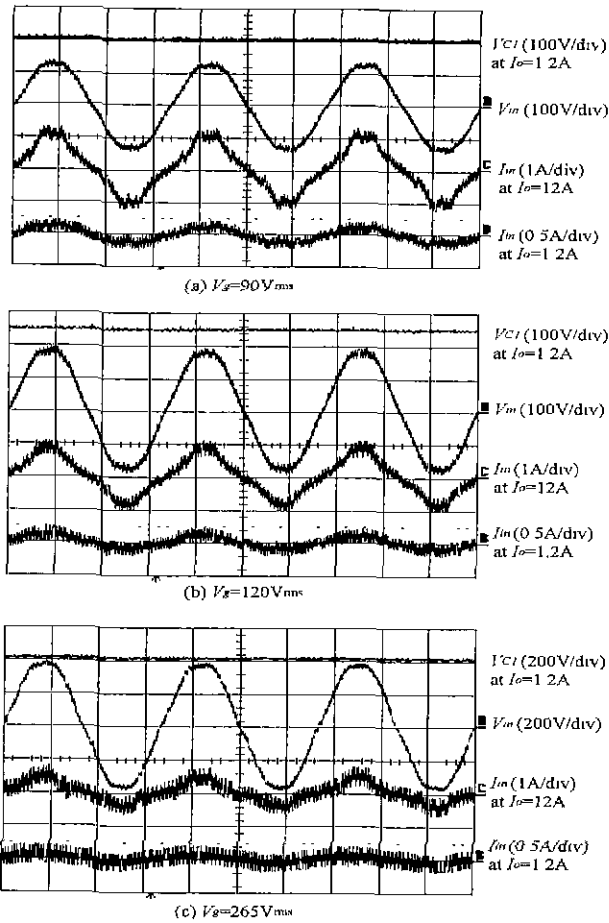


Fig. 5 The measured line voltage/current and link voltage waveforms

output is implemented. The experimental results show that the converter meets IEC61000-3-2 class D limits with a sufficient margin and the power factor is above 0.96 under the universal line condition in case that the load is higher than 30%. The maximum measured efficiency is about 81% and the maximum link voltage is 447V

REFERENCES

[1] J. Y. Lee, G. W. Moon, and M. J. Youn, "Design of a power-factor-correction converter based on half-bridge topology," *IEEE Trans. Ind. Applicat.*, Vo. 46, no. 4, pp. 710-723

[2] M. M. Jovanovic, D. M. Tsang, and F. C. Lee, "Reduction of voltage stress in integrated high-quality rectifier-regulators by variable frequency control," in *IEEE Applied Power Electronics Conf.*, 1994, pp. 569-575

[3] J. Qian, Q. Zhao, and F. C. Lee. "Single-stage single-switch, power factor correction(S<sup>4</sup>-PFC)

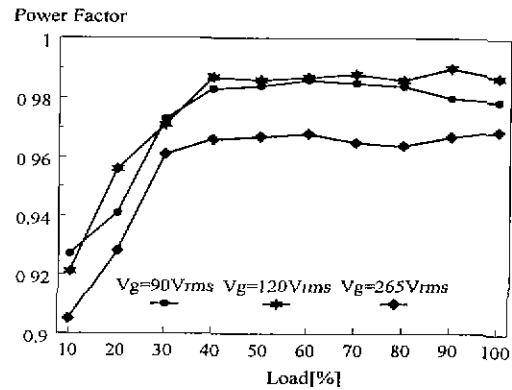


Fig. 6 The measured power factor under line and load variations

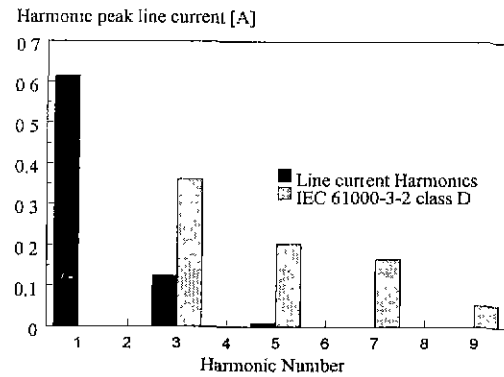


Fig. 7 IEC 61000-3-2 class D limits and the measured line current harmonics

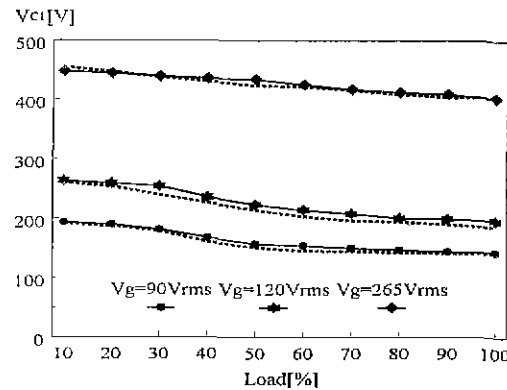


Fig. 8 The measured and calculated(dotted line) link capacitor voltage stresses under line and load variations

AC/DC converters with DC bus feedback for universal line applications," in *VPEC '97 seminar proceeding*, 1997, pp. 29-35

[4] M. Daniele, P. K. Jain, and G. Joos, "A single-stage power-factor-corrected AC/DC converter," *IEEE Tans. Power Electron.*, Vol. 14, no. 6, pp. 1046-1055, 1999.