FPAG를 위한 최적화된 기술 매핑에 관한 연구

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A Study on Optimized Technology Mapping for FPGA

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Abstract

We are studied on the performance optimized synthesis and mapping of design on to one or more FPGA device. our multi-phased approach optimized the key parameters that affect performance by adequately modeling the impact on wire length, routability, and performance during technology mapping to produce designs that have high performance and high routability potential.

I. Introduction

In this paper we are studied on the performance optimized mapping of design on to one or more FPGA Device. Our goal in the technology mapping phase is to arrive at a design implementation which has the best performance and routing potential.[1][2][3] In order to achieve high performance implementations it is important to minimization with minimal increases in area and interconnections and thereby indirectly improves the quality of placement and routing to promote smaller wire delays in general. In addition, we propose to complement the depth mapping with minimum critical wire lengths using timing driver pre-placement to derive placement and routing constraints.

II. Approach to performance optimized technology mapping.

In this paper we propose a two phased approach for technology mapping shown in Figure1.The input network is first conditioned through two-level and multi-level optimization using logic optimization[4]. The input network consists of primitive gates. In the first phase we perform simultaneous depth and area minimized technology mapping. In the second phase we perform a timing driver placement to minimize critical wire lengths and to prevent alternate critical path. The outcome of the second phase is a set of placement and routing constraints which are than phased along with the mapped design to Xilinx's FPGA place and route tools[5].

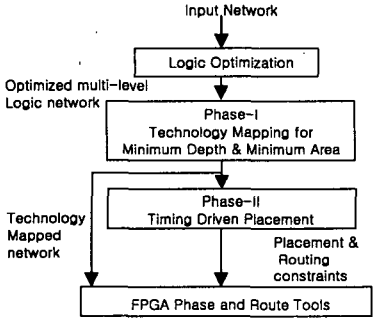

Fig1. Performance of optimized technology mapping

The chortle-d approach[1] succeeded in significantly reducing the depth of logic, but, at a significant cost in terms of number of LUTs and number of connections. Chortle-d demonstrated that their approach produced mapping with optimal depth when the input is fan-out free tree and when the number of inputs to the LUT[3] is less than or equal to 6. In the first phase the network depth is minimized by controlling critical nodes into their fan-outs and re-synthesizing the collapsed node with fewer number of levels using a number of decomposition techniques such as Roth-Karp, co-factoring AND / OR decompositions, and algebraic decompositions. The second phase used logic re-synthesis during a simulated annealing based timing driver placement to minimize critical paths delays. The results from the first phase of mis-pga(delay) were significantly better in terms of area and number of connections, but yielded larger number of levels, the smaller area and connections in designs produced by mis-pga(delay) resulted in factor designs after place and route compared to chortle-d.

Ⅲ. Approach to performance directed technology mapping.

A combinational input network for technology mapping consisting of a set of Boolean functions may be looked upon as a directed acyclic graph(DAG) G=(V.E). The articles(or nodes) are the primitive Boolean operators and the directed edges(from the output of a node to an input of another node) are the connections between operators. Edges also carry phase information indicating whether an operator s output must be complemented. A primary output node has no outgoing edges and a primary input node has no incoming edges. The mapping process adding one or more look-up-tables (LUT) to each node visited to realize the node s function. It showed be noted that our assumption of a combinational logic network as an input to technology mapping is not a limitations. When we are giver a general Boolean network consisting of sequential elements, the sequential elements are ignored during the technology mapping process, after

the mapping of the combinational logic is completed, the sequential elements are either assigned to existing LUTs or to new LUTs as necessary. For the duration of technology mapping the inputs to the sequential elements are treated as primary outputs and the outputs of sequential elements are treated as primary inputs. The performance of a design mapped on to an FPGA device is governed:

1.Clique partitioning based technology mapping

The mapping process involves a post-order traversal of the input network(or Directed Acyclic Graph G=(V.E). At each node v visited in post-order our goal is to minimize the number of LUTs(Look Up Tables) required to realize the function of node v. In this process we identify an efficient decomposition of v and merge as many of v's fan-in LUTs as possible to realize the fanction of v.

The inputs to Algorithm DM consist of the starting network to be mapped and also the required depth of logic in mapped network the goals of Algorithms DM are;.Achieve technology mapping with specified depth whenever possible or minimize the depth when the specified depth requirements can not be met. Minimize the number of LUTs and the number of interconnections which in influence wire lengths and the wire delays. This Algorithm DM can produces level efficient designs with fewer number of LUTs and fewer connections which in turn improve the potential the potential to minimize wire lengths during placement and routing.

IV. Conclusion

In this study we address the problem of performance optimized synthesis of designs on to one or more FPGAs. Our multi-phased approach optimizes the key parameters that affect performance by adequately modeling the impact on wire length, routability, and performance during technology mapping to produce designs that have high performance and high routability potential. From this approach we have developed novel techniques for technology mapping which produce designs with high performance and routability potential. Our approach was to perform a simultaneous depth and area minimized technology mapping in the first phase so that logic depth of the network in minimized with minimal area penalty. This strategy of controlling the area costs during depth minimization promotes good placement and routing configurations and does not adversely impact the wire lengths and wire delays that can be achieved. The second phase of our approach involved a timing driven placement to control the critical wire lengths and generate placement and routing constraints that could be used with the actual FPGA place and route tools.

Reference

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