Multi-Operand Radix-2 Signed-Digit Adder using Current Mode MOSFET Circuits

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Abstract: This paper describes a novel multi-operand radix-2 signed-digit(SD) adder. The novel multi-operand addition algorithm can eliminate carry propagation chain by dividing the input operands into even place part and odd place part, and adding them each. The multi-operand adder with this algorithm can add six operands in parallel, and is faster than the ordinary method of SD adder binary tree. A hardware model for proposed adder is shown which is implemented by the current-mode MOSFET circuit technology. Simulations have been made by SPICE in order to verify the function of the proposed circuit.

1. Introduction

As compared with ordinary binary logic, signed-digit logic (redundant number logic)[1] which is a kind of multiple-valued logic have the great advantage in the addition operation because of eliminating carry propagation chain. Therefore the total parallel adder of which the addition speed is independent of the number of digits can be constructed. By utilizing this advantage, many applications such as fast multiplier are reported[2]. Especially, radix-2 signed-digit logic (so called as redundant binary logic) system and radix-4 signed-digit logic system are easy to use with ordinary binary system, so its practicability is high.

Considering the applications of this signed-digit adder to the multiplier, digital filter and so on, it is necessary to add many operands simultaneously. For example, a multiplication of n-digits multiplier and n-digits multiplicand needs the n-operands addition fundamentally, or some of modern digital filters need the several hundred operands addition. So far, they have been realized by binary tree structure of 2-operands signed-digit adder. This structure needs the many circuit elements and addition time proportionate to $O(\log_2 m)$ in case of m-operands addition, it is not efficient in respect of both power consumption and operating speed.

We propose a novel multi-operand radix-2 signed-digit addition algorithm in this paper. By using this algorithm, the feature that the operating delay is independent of the number of digits is kept, concurrently a multi-operand addition can be realized. The principle of this algorithm is that input operands are divided into even place part and odd place part, and they are added separately. It can eliminate carry propagation chain also in case of multi-operand addition. The multi-operand adder with this algorithm can add six operands in parallel, by the delay time proportionate to $O(\log_3 m)$, and is faster than the ordinary method of binary tree. In addition, circuit elements also decrease, so that power consumption is also smaller.

2. SD addition algorithm

The expression of n-digits SD number $X = (x_{n-1}x_{n-2}\cdots x_0)_{2SD}$ is represented as

$$\begin{aligned} X &= (x_{n-1}x_{n-2}\cdots x_1x_0)_{2SD} \\ &= \sum_{i=0}^{n-1} x_i \cdot 2^i \end{aligned}$$

where $x_i \in \{\bar{1}, 0, 1\}$ and $\bar{1} = -1$.

An addition between two SD number, X and Y, is performed in every place (i-th place) by following three steps:

$$\begin{aligned} \textbf{step1:}\quad & z_i = x_i + y_i \\ \textbf{step2:}\quad & 2c_i + w_i = z_i \\ \textbf{step3:}\quad & s_i = w_i + c_{i-1} \end{aligned}$$

where z_i is arithmetic sum, w_i is interim sum, c_i is carry and s_i is final sum of i-th place, respectively they take the values as follows:

$$\begin{aligned} x_i, y_i &\in \{\bar{1}, 0, 1\} \\ z_i &\in \{-2, -1, 0, 1, 2\} \\ w_i, c_i, s_i &\in \{\bar{1}, 0, 1\} \end{aligned}$$

There are several combinations of $\{c_i, w_i\}$ depending on the value of z_i by the redundancy of SD number. If proper combination of $\{c_i, w_i\}$ is selected in compliance with the possibility of a carry from previous($(i-1)$-th) place, always carry propagation chain can be eliminated, so that the total parallel addition can be realized. The possibility of a carry can be decided by a sign of z_{i-1}. Table 1 shows the selection rule of the such combination.

Table 1: Selection rule of interim sum and carry for 2-operands SD addition.

	$z_{i-1} > 0$		$z_{i-1} \leq 0$	
z_i	c_i	w_i	c_i	w_i
2	1	0	1	0
1	1	$\bar{1}$	0	1
0	0	0	0	0
−1	0	$\bar{1}$	$\bar{1}$	1
−2	$\bar{1}$	0	$\bar{1}$	0

3. Principle of Multi-Operand SD Addition

Multi-operand SD addition is an addition among more than three operands. In this case, the carry may transfer from i-th place to not only $(i+1)$-th place but also more than $(i+2)$-th place. The carry propagation chain is unavoidable even SD addition.

In order to overcome this shortcomings, we propose a novel multi-operand SD addition algorithm. The principle of this algorithm is that input operands are divided into even place part and odd place part, and they are added separately. There are places whose interim sums are zero in every other place, consequently it can eliminate carry propagation chain even multi-operand addition. Fig. 1 shows the way to divide the input operands, where $K, L, \ldots, P$ are input operands. Finally, two operands, that are the sum results as even part addition and odd part addition, are added each other by ordinary 2-operand SD adder, as shown in Fig. 2.

In this algorithm, it is considered that the carries transfer from i-th place to only $(i+1)$-th and $(i+2)$-th place. In other words, i-th place arithmetic sum must be represented as three digits SD number. Therefore, considering a carry from $(i-2)$-th place, maximum sum of i-th place is $(1\,1\,0)_{2SD} = 6$. After all, multi-operand adder with this algorithm can add six

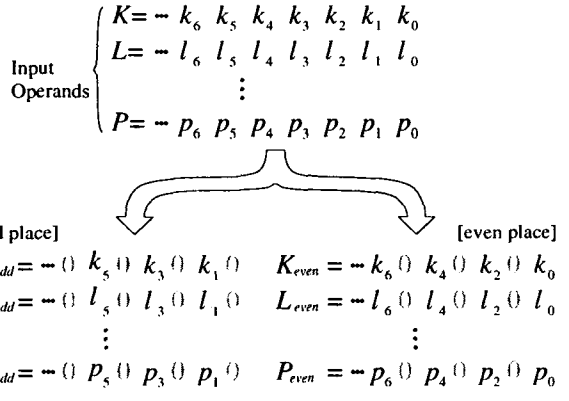

Figure 1: The way to divide the input operands.

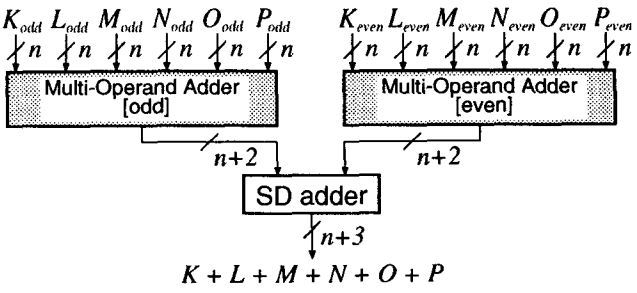

Figure 2: Block diagram of proposed multi-operand SD adder.

operands in parallel.

The addition steps in every place is as follows:

$$\textbf{step1:}\quad z_i = k_i + l_i + m_i + n_i + o_i + p_i$$
$$\textbf{step2:}\quad 2^2 d_i + 2c_i + w_i = z_i$$
$$\textbf{step3:}\quad s_i = w_i + d_{i-2}$$

where z_i is arithmetic sum, w_i is interim sum, c_i is carry to $(i+1)$-th place, d_i is carry to $(i+2)$-th place, and s_i is final sum of i-th place, respectively they take the values as follows:

$$k_i, l_i, m_i, n_i, o_i, p_i \in \{\bar{1}, 0, 1\}$$
$$z_i \in \{-6, -5, \ldots, 0, \ldots, 5, 6\}$$
$$w_i, c_i, s_i \in \{\bar{1}, 0, 1\}$$

Table 2 shows the selection rule. In this table, signal e_{i-2} represents the information of possibility whether carry exists or not, and whether carry is 1 or $\bar{1}$, from $(i-2)$-th place. It is defined as:

$$e_i = \begin{cases} 1 & \text{where} \quad z_i > 0 \\ 0 & \text{where} \quad z_i \leq 0 \end{cases} \tag{1}$$

Fig. 3 shows a block diagram of multi-operand adder that realizes the addition steps and the Table 2 described above. Also from this figure, it is clear that the operating delay is independent of the number of digits, so that a parallel multi-operand addition can be realized.

4. MOSFET Circuit Design and Simulation Results

We have designed this multi-operand adder by using current mode MOSFETs technology[4, 5]. Since the current mode circuits can express the sign by current direction, it is very suitable to implement the SD logic system using the logic value of $\{\bar{1}, 0, 1\}$. Furthermore, it has great advantage in realization of the summation on proposed multi-operand adder, because current mode MOSFET circuits can perform the summation of input signals as "wired summation." Therefore actual circuit can be implemented by less circuit elements. The proposed current mode circuit consists of

Table 2: Selection rule of interim sum and carry for multi-operand SD addition.

		$e_{i-2}=1$			$e_{i-2}=0$		
z_i	e_i	d_i	c_i	w_i	d_i	c_i	w_i
6	1	1	1	0	1	1	0
5	1	1	1	$\bar{1}$	1	0	1
4	1	1	0	0	1	0	0
3	1	1	0	$\bar{1}$	0	1	1
2	1	0	1	0	0	1	0
1	1	0	1	$\bar{1}$	0	0	1
0	0	0	0	0	0	0	0
−1	0	0	0	$\bar{1}$	0	$\bar{1}$	1
−2	0	0	$\bar{1}$	0	0	$\bar{1}$	0
−3	0	0	$\bar{1}$	$\bar{1}$	$\bar{1}$	0	1
−4	0	$\bar{1}$	0	0	$\bar{1}$	0	0
−5	0	$\bar{1}$	0	$\bar{1}$	$\bar{1}$	$\bar{1}$	1
−6	0	$\bar{1}$	$\bar{1}$	0	$\bar{1}$	$\bar{1}$	0

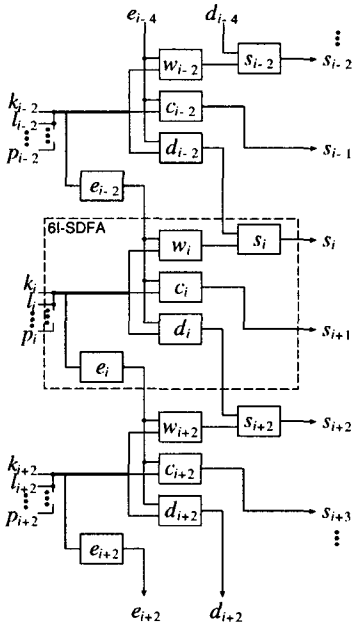

Figure 3: Block diagram of multi-operand adder for proposed algorithm.

circuit elements such as threshold detector circuits and current mirror circuits as shown in Fig 4. The threshold detector circuit is to produce an digital output signal depending if input signal exceeds a defined threshold value or not. The value of threshold can be realized by the channel width of the threshold detector transistor. The current mirror circuit is to produce any copies of input signals, to determine the current direction and to weight integer.

Fig. 5 shows the 6I-SDFA circuit constructed by using such circuit elements. "6I-SDFA" means a 6-input SD full-adder indicated by dashed line in Fig. 3.

In order to verify the function of the proposed multi-

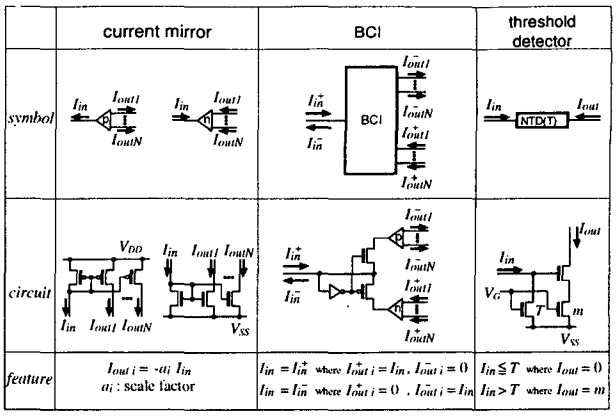

Figure 4: Circuit elements for current mode MOSFET circuits.

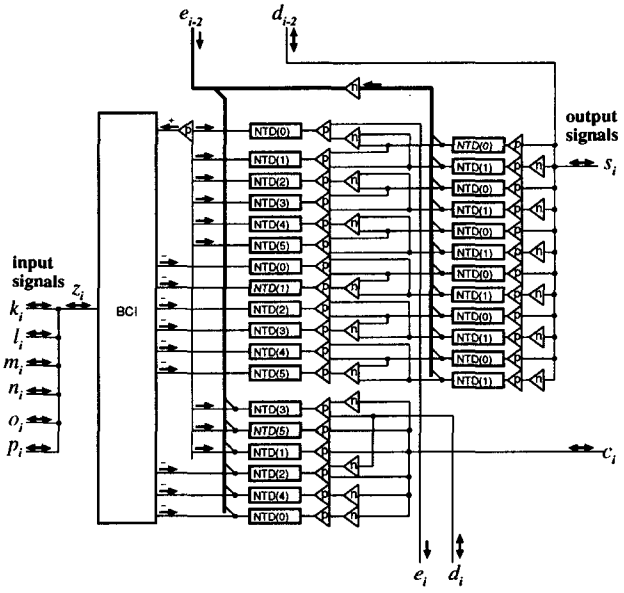

Figure 5: 6-inputs SD full adder (6I-SDFA) circuit.

operand SD adder, simulations have been made by SPICE. We have used a model parameter with 0.5 micron rules technology. Unit current corresponding to logical value of "1" is 40[μA]. Fig. 6 shows one example of simulation results of 8bit/6-operands SD addition by using proposed 6I-SDFA. These results are obtained by following input patterns:

$$K = (1\,1\,\bar{1}\,\bar{1}\,1\,0\,\bar{1}\,\bar{1})_{2SD} = (149)_{10},$$
$$L = (1\,\bar{1}\,1\,0\,0\,0\,\bar{1}\,\bar{1})_{2SD} = (93)_{10},$$
$$M = (1\,0\,1\,0\,\bar{1}\,0\,0\,1)_{2SD} = (153)_{10},$$
$$N = (0\,1\,0\,0\,1\,1\,1\,0)_{2SD} = (78)_{10},$$
$$O = (1\,0\,0\,1\,\bar{1}\,0\,\bar{1}\,0)_{2SD} = (134)_{10},$$
$$P = (0\,0\,0\,\bar{1}\,\bar{1}\,0\,1\,\bar{1})_{2SD} = (-23)_{10}$$

and even part and odd part addition results are:

$$S_{even} = (0\,0\,0\,1\,0\,\bar{1}\,0\,1\,\bar{1}\,0)_{2SD} = (50)_{10}$$

$$S_{odd} = (1\,0\,0\,0\,1\,\bar{1}\,1\,1\,1\,0)_{2SD} = (534)_{10}$$

respectively. Therefore, from an equation as $149+93+153+78+134-23=50+534=584$, it is clear that the right operation results are obtained.

In this result, total delay time of the multi-operand adder is 16.8[ns] independing on the number of digits. It is 31.7% faster than ordinary circuit using 2-operand SD adders binary tree. Total power consumption is 34.5[mW], it is 35.4% fewer. The number of transistors is 2888, it is 31.4% fewer. From these results, proposed adder has great advantages over the ordinary adder.

5. Conclusion

A novel multi-operand radix-2 signed-digit addition algorithm has been proposed. Its circuit implementation by using current-mode MOSFET circuits has been also described in detail, and simulations have been made. From these results, proposed adder is 31.7% faster than ordinary system, and its power consumption is 35.4% fewer in case of 8bit/6-operands SD addition. These results show that proposed algorithm is superior in the point of both speed and power consumption. Moreover, the more number of operands to add, the faster this circuit works than ordinary system. It enables the construction of many bits multiplier and faster digital filters.

Acknowledgements

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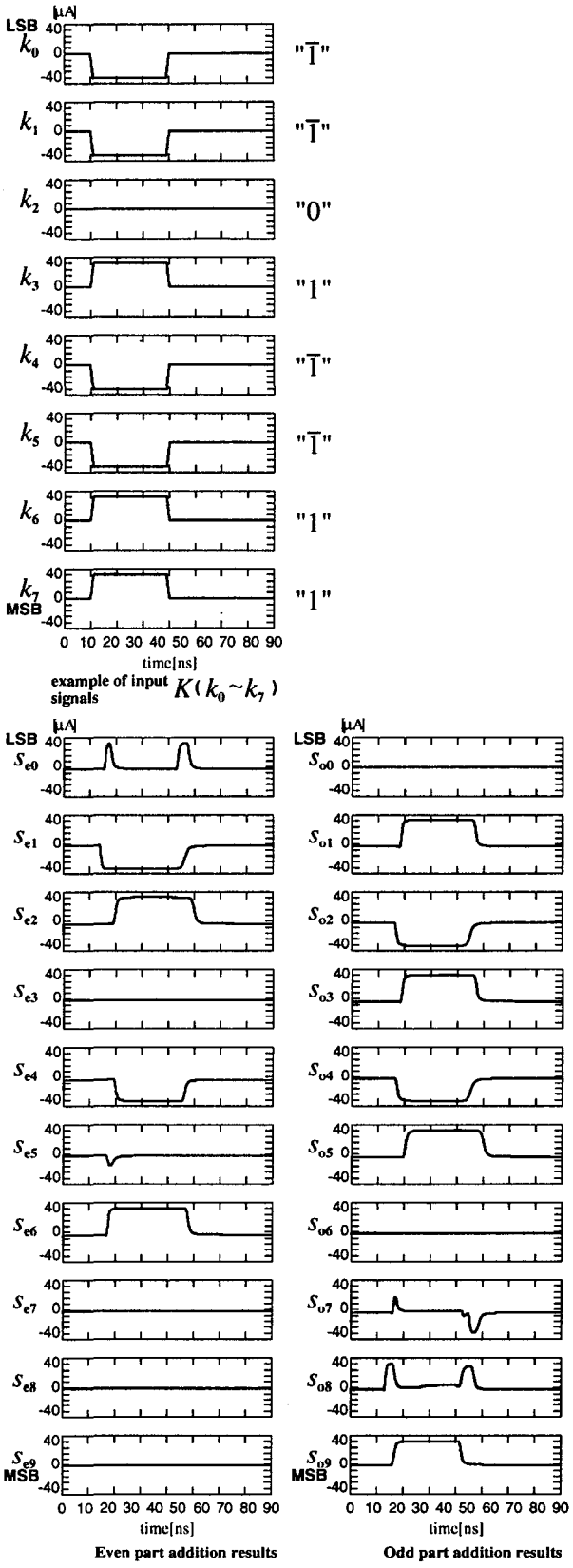

Figure 6: One example of simulation results of 8bit/6 operands SD addition. note About input operands, only K is shown, other inputs are omitted.