A DESIGN OF MULTIPLE-VALUED SOFT-HARDWARE LOGIC CIRCUITS USING NEURON MOS TRANSISTOR

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Abstract: A level of integration will increase, if the number of elements of the circuit can be reduced. We aim to design the circuit of the new system for any further integration by using Neuron MOS Transistor.

In this paper, we consider to introduce Soft-Hardware Logic and multiple-valued logic to the design methods for reducing the number of elements and inner wiring. We have designed 4-valued add-subtracter circuit using above logic. We discuss the design methods, features, and characteristics of this circuit by SPICE simulation.

1. Introduction

The integrated circuit design by using CMOS device has to be solved an important problem. That is related to the integration of the circuit. Level of circuit integration was increasing rapidly during the past several years. But, any further integration becomes difficult. It will be thought increasing in the number of inner wiring inside the circuit caused by the increase in a level of integration and the complication of the wiring in this factor.

It can be solved this problem if the number of elements of the circuit can be reduced. So, we paid attention to Neuron MOS Transistor. The circuit of the new system that contributes to the improvement of the above problem by using this device as the basic element can be constructed. We designed 4-valued add-subtracter by using soft-hardware logic and the multiple-valued logic.

2. Neuron MOS Transistor

The neuron MOS transistor is shown in Fig. 1. The basic construction of the neuron MOS transistor is ordinary MOSFET.

The neuron MOS transistor consists of electrical floating gate and multiple input gates. These input gates are capacitively coupled to the floating gate.

The ON and OFF operation of the neuron MOS transistor is controlled by whether the floating-gate potential is high or not than the threshold voltage V_{TH} of the transistor. The electrical potential Φ_F of the floating gate is described by

$$\phi_F = \frac{C_1V_1 + C_2V_2 + \cdots\cdots C_nV_n}{C_0 + C_1 + C_2 + \cdots C_n}.$$

C_0 is the capacitive coupling coefficient between the floating-gate and the substrate.

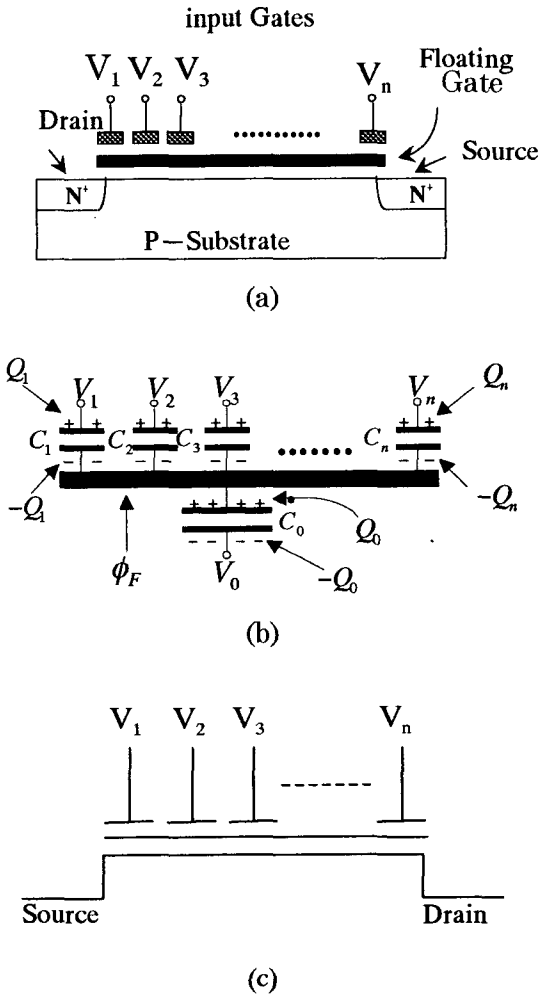

Fig.1. Neuron MOS transistor: (a) basic construction. (b) Relationship among terminal voltages and capacitance coupling coefficients. (c) Symbol representation.

3. The configuration of the neuron MOS transistor

3.1 Neuron MOS inverter

The neuron MOS inverter employing CMOS configuration is illustrated in Fig. 2. The relationship of the output V_{out}, the threshold voltage V_{TH} and floating-gate potential Φ_F is shown as Table 1 and Fig.3.

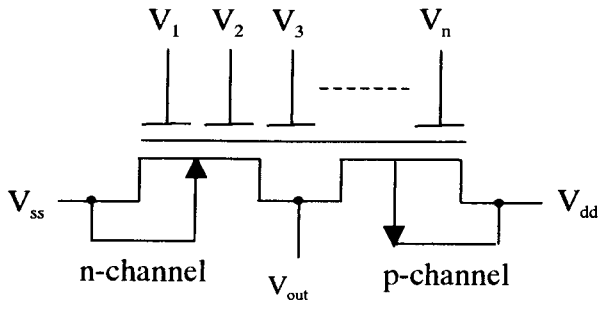

Fig.2. Neuron MOS inverter

Table 1. The relationship of Φ_F, V_{TH} and V_{out}

Φ_F , V_{TH}	V_{out}
$\Phi_F < V_{TH}$	High
$\Phi_F > V_{TH}$	Low

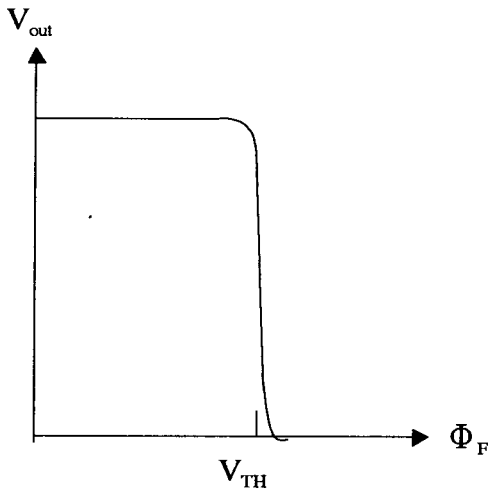

Fig.3. The relationship of V_{out} and Φ_F.

3.2 Neuron MOS Source-Follower Circuit

The complementary neuron MOS source-follower circuit can be constructed by the parts of channels at the inverter circuit in Fig. 2 change as that shown in Fig.4.

The floating-gate potential Φ_F defined in chapter 2 is sum of multiplication the input signals and capacitive coupling coefficient of the respective gate. This circuit directly read out the floating-gate potential in V_{out} is given by

$$V_{out} = \Phi_F .$$

For instance, The output of 3-inputs circuit illustrated in Fig.5, in which C_1: C_2: C_3=1:1:1, becomes like as Fig. 6.

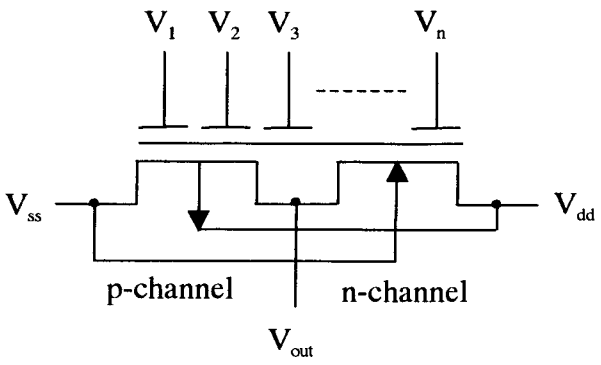

Fig.4. A complementary neuron MOS source-follower circuit.

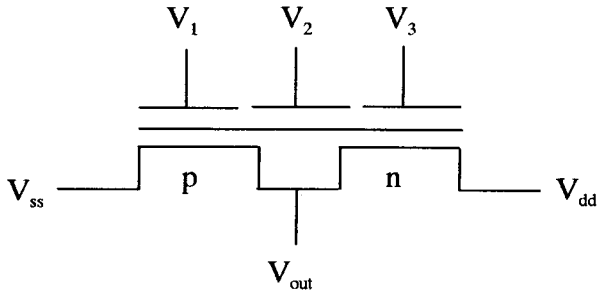

Fig.5. 3-inputs source-follower circuit

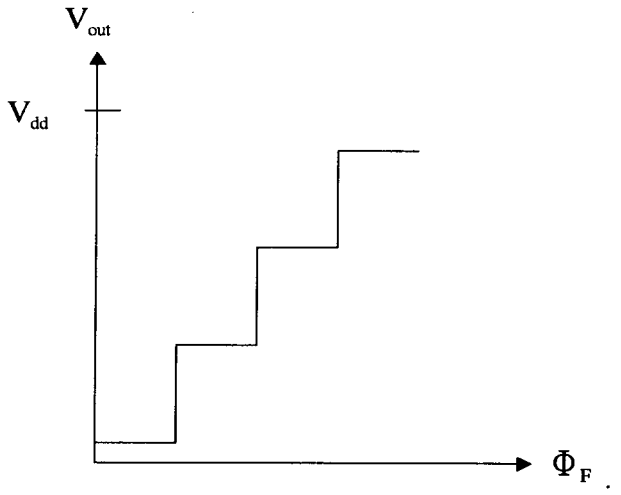

Fig.6. The output of 3-inputs circuit

4. SOFT-HARDWARE LOGIC

A soft-hardware logic (SHL) circuit can be constructed by using the neuron MOS transistor. The construction of soft-hardware logic circuit is shown in Fig.7.

SHL is the circuit that realized multiple function on one hardware. These functions can be changed freely by the signal inputted to the control terminal of this hardware in real time. And, when it is changed, it doesn't need to do modification inside that hardware at all.

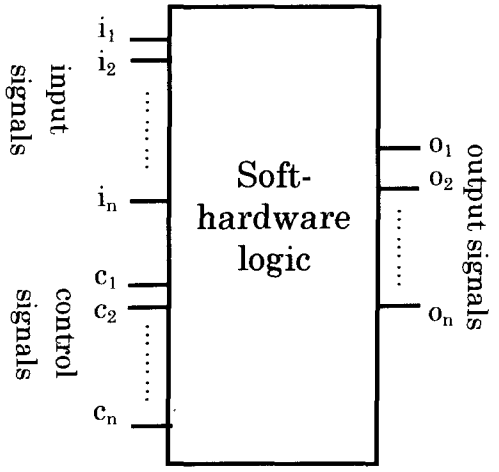

Fig.7.Soft-hardware logic.

5. MULTIPLE-VALUED LOGIC

Multiple-valued logic uses a multiple-valued signal, such as 4-valued signal and 10-valued signal, in addition to digital signal.

Though the output of the neuron MOS transistor is surely digital value, the each signal inputted to multiple input terminal use both digital value and multiple value. Furthermore, multiple value can be outputted when a source follower circuit which outputs the weighted average of signals added to input terminals is composed of the neuron MOS transistor. So, the neuron MOS transistor can make use of this logic easily.

The amounts of information transmitted on 1-wiring are on increase by designing a circuit with this system. It is said that numbers of inner wiring decreases.

The construction realized the multiple-valued logic is shown in Fig. 8. This circuit consists of neuron MOS source-follower and neuron MOS inverters f_1 ,f_2 ,····· f_n for controlling the source-follower. The differences of the neuron MOS inverters are C_1 , C_2 , ····· C_n .

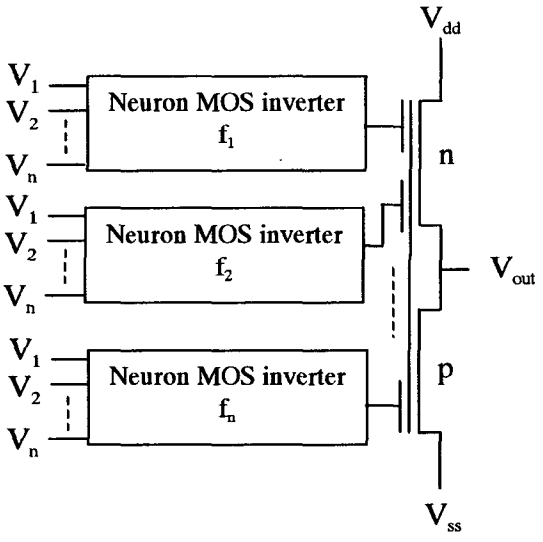

Fig. 8. The multiple-valued logic

6. 4-VALUED ADD-SUBTRACTER

4-valued add-subtracter uses 4-valued signal. These values are each value that a standard voltage was divided into three levels, and 0V. The functions of the addition and the subtraction are composed by one hardware. Either function can be chosen only at the control signal without reconstructing the circuit.

The construction of 4-valued add-subtracter is shown in Fig.9.

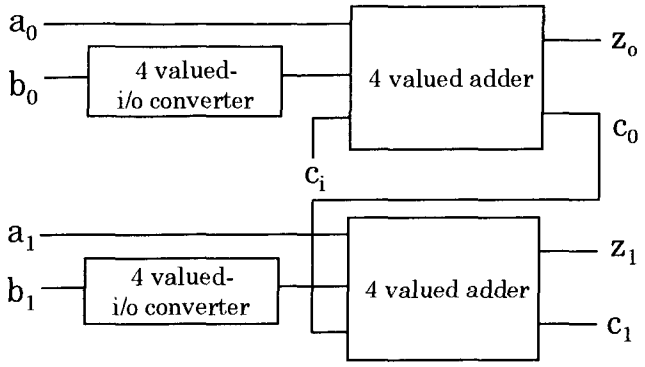

Fig.9. 4-valued add-subtracter.

Basic composition consists of two parts. There are 4-valued adder and the circuit to control the function of the addition and the subtraction.

This circuit is i/o converter that an input signal is changed into the desired output signal by the control signal (Fig.10).

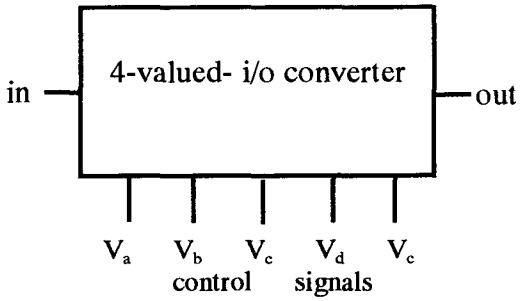

Fig.10. 4-valued- i/o converter

The output stage of the 4-valued-i/o converter shown in Fig.11 is 2-inputs (L_1 , L_2) neuron MOS source-follower , in which the ratio of C_1 and C_2 is 2 : 1 .

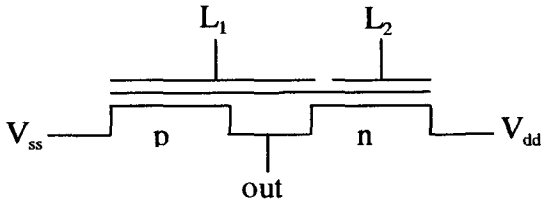

Fig.11. 2-inputs (L_1 , L_2) neuron MOS source-follower

The input stage neuron MOS circuit is shown in Fig. 12 (a) or (b) has L_1 or L_2 as output .

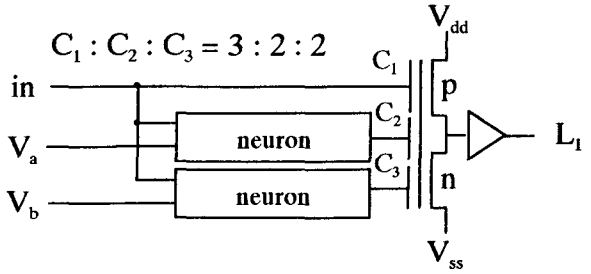

Fig. 12 (a). L_1 controller

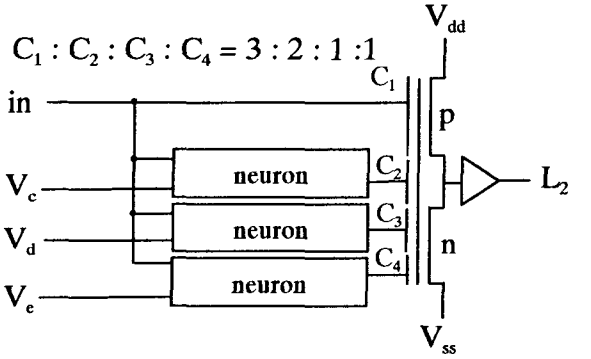

Fig. 12 (b). L_2 controller

The neuron circuit parts in Fig. 12 (a) and (b) are illustrated in Fig. 12 (c).

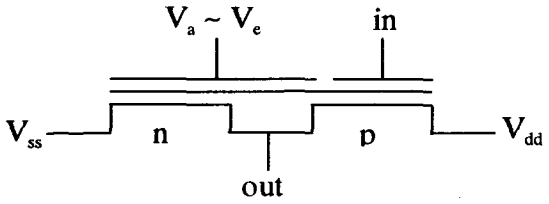

Fig. 12 (c) . Neuron circuit parts.

The input and output relations of the i/o converter are decided as Table 2(a) to take the addition function. In other words, it is the change-less circuit, which doesn't change the input signal.

Table 2. i/o relations.

(a) addition

in	out
0	0
1	1
2	2
3	3

(b) subtraction

in	out
0	3
1	2
2	1
3	0

The input and output relation of the i/o converter becomes as Table 2(b) to take a subtraction function. This input and output relation shows the function which is equivalent to complementer. The i/o converter changes the input signal b_1 into complement signal.

The choice of these functions can be carried out setting the control signal values. Table 3 is relation of control signal values and functions of addition or subtraction.

Table 3. control signal values.

control signals	addition (V)	subtraction (V)
V_a	0.0	2.5
V_b	5.0	2.5
V_c	2.5	4.2
V_d	0.0	0.8
V_e	5.0	0.8

Controlling the change of the input signal by the i/o converter by using the control signal changes the settlement of the addition and the subtraction. Table 4 is the simulation result of the 4-valued add-subtracter.

Table 4 . The simulation result

input (4 levels) A	input (4 levels) B		control signals (V)					output	
$a_0\ a_1$	$b_0\ b_1$	c_i	V_a	V_b	V_c	V_d	V_e	$z_0\ z_1$	functions
1 2	0 3	0	0.0	5.0	2.5	0.0	5.0	2 1	addition A + B
1 3	1 2							3 1	
2 1	1 2							3 3	
2 2	0 3							3 1	
2 3	2 2	1	2.5	2.5	4.2	0.8	0.8	0 1	subtraction A - B
3 1	1 2							1 3	
3 2	0 3							2 3	
3 3	1 2							2 1	

6. CONCLUSIONS

At present, it has been getting difficult to do any further integration in the integrated circuit design. We decide to use the neuron MOS transistor as the basic element from the viewpoint of whether the number of elements can't be decreased to improve this problem. We have designed 4-valued add-subtracter by using soft-hardware logic and the multiple-valued logic.

References

[1] T . Shibata and T . Ohmi, "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations" *IEEE Trans. Electron Devices, Vol. 39, No.6,june 1992.*

[2] T . Shibata and T . Ohmi, "Neuron MOS Binary-Logic Integrated Circuits. Part 1 : Design Fundamentals and Soft-Hardware-Logic Circuit Implementation" *IEEE Trans. Electron Devices, Vol. 40, No.3,March 1993.*

[3] T . Shibata and T . Ohmi, "Neuron MOS Binary-Logic Integrated Circuits. Part 2 : Simplifying Techniques of Circuit Configuration and their Practical Applications" *IEEE Trans. Electron Devices, Vol. 40, No.5,March 1993.*

[4] T . Shibata and T . Ohmi, "Neuron MOS Voltage-Mode Circuits Technology for Multiple-Valued Logic" *IEICE Trans. Electron Devices, Vol. E76-C, No.3,March 1993.*