Design of a High-Dimensional Discrete-Time Chaos Circuit with Array Structure

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Abstract

In this paper, a discrete-time S-dimensional chaos circuit ($S = 1, 2, 3, 4, \ldots$) with array structure is proposed. By employing array structure which consists of 1-dimensional chaos circuits, the proposed circuit can achieve long working-life. This feature is favorable to exploit as a building block of chaos application systems to get into home electric appliances. Furthermore, the proposed circuit synthesized using switched-current (SI) techniques is suitable for integration. Concerning the proposed circuit, SPICE simulations are performed. SPICE simulations showed that the proposed circuit can generate the chaotic signals in spite of the fault of the building blocks of the proposed circuit. The proposed circuit is integrable by a standard BiCMOS technology.

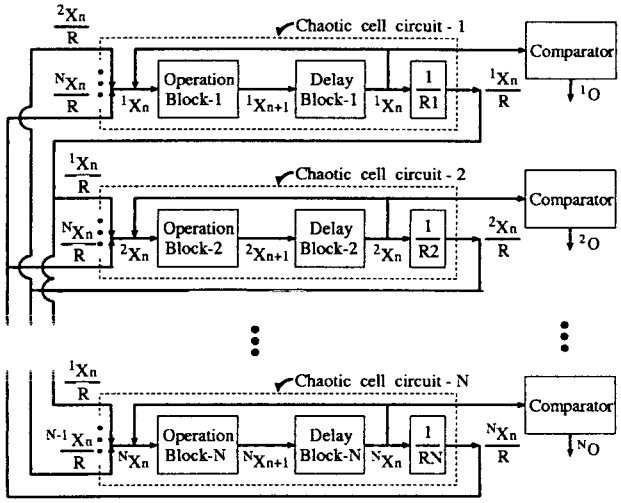

Fig.1 Block diagram of the proposed circuit.

1 Introduction

In the field of engineering, the applications of chaos attract many researchers' attension, for example, chaos-based communication systems, chaotic neural networks, social behavior simulations, etc. [1],[2]. To realize these application systems, the integrated chaos circuits are required. Among others, high-dimensional chaos circuits are useful as an experimental tool for observation of chaotic behavior since they can demonstrate more various bifurcation modes than that of 1-dimensional chaos cirucits. Furthermore, chaos application systems such as social behavior simulations require high-dimensional chaotic signals. For this reason, several high-dimensional chaos circuits have already been proposed [3],[4]. Most of these chaos circuits are 3-dimensional continuous-time chaos circuits. Although high-dimensional chaotic signals can be generated by these continuous-time chaos circuits, we focused on a discrete-time chaos circuits. Different from continuous-time chaos circuits, discrete-time chaos circuits can be realized in a 1-dimensional form. Furthermore, compared with continuous-time chaos circuits, the chaotic behavior of the 1-dimensional chaos circuits is simple.

In this paper, a discrete-time S-dimensional chaos circuit ($S = 1, 2, 3, 4 \ldots$) with array structure is proposed. In the proposed circuit, N 1-dimensional chaos circuits ($N > S$) are arrayed redundantly. A high-dimensional chaos circuit is constructed with these 1-dimensional chaos circuits. Since 1-dimensional portions which are at fault can be detected by exploiting the characteristics of the 1-dimensional chaos circuit, the proposed circuit can reconstruct the high-dimensional chaos circuit by using redundant 1-dimensional chaos circuits. Hence, the proposed circuit can achieve long working-life. Furthermore, the proposed circuit synthesized using switched-current (SI) techniques is suitable for integration. Concerning the proposed circuit, computer simulations are performed.

2 Circuit Structure

Figure 1 shows the general circuit architecture of the proposed circuit. The proposed circuit consists of N comparators and N building blocks which are called chaotic cell circuits. The dynamics of the proposed

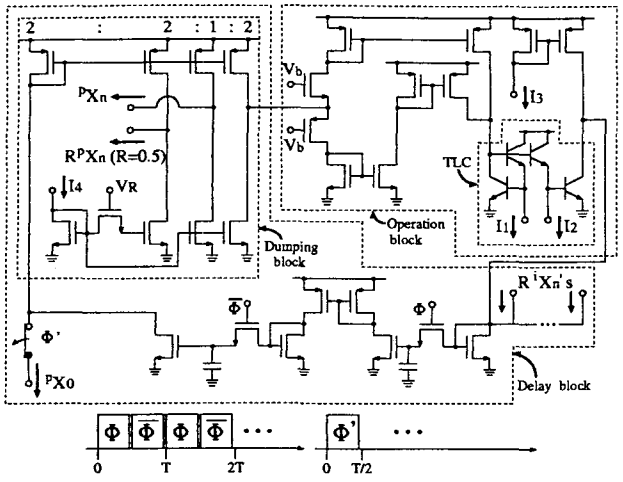

Fig.2 Chaotic cell circuit designed by using SI techniques.

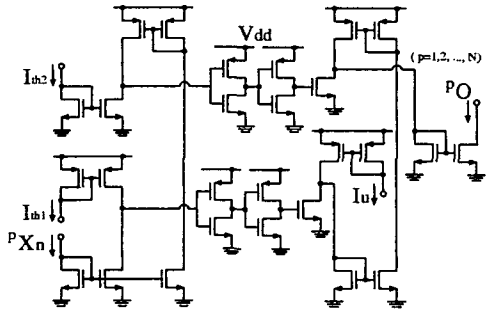

Fig.3 Comparator designed by using current-mode techniques.

circuit is based on the following equation:

$$^{P}X_{n+1} = F(^{P}X_n) + \sum_{i=1}^{N} R\ ^{i}X_n, \quad (i \neq p) \quad (1)$$

where F(·) is a nonlinear function and R is a damping factor. In the chaotic cell circuit, the operation F(·) in Eq.(1) is realized by the operation block. And a unit delay is realized by the delay block. In the comparator, fault of the chaotic cell circuits is detected. Figure 2 shows the proposed chaotic cell circuit designed by using switched-current (SI) techniques. The synthesis of the proposed SI chaos circuit is based on the following equation:

$$\begin{aligned} ^{P}X_{n+1} &= F(^{P}X_n) \\ &= 1 - {}^{P}A|^{P}X_n| + \sum_{i=1}^{N} R\ ^{i}X_n, \quad (i \neq p) \quad (2) \end{aligned}$$

where ^{P}A is a parameter. The operation block in Fig.2 consists of translinear multiplier/divider circuit (TLC) and current mirrors. The delay block in Fig.2 is constructed with SI track & hold circuits.

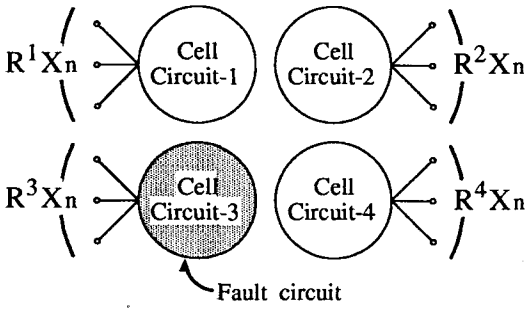

Fig.4 SPICE simulated circuit composed of 2 × 2 chaotic cell circuits.

The operation block functions as $F(^{P}X_n)$. In this block, the parameter ^{P}A is realized by the current ratios I_1/I_2 in the multiplier/divider circuit. Although the multiplier/divider circuit can be constructed with MOSFET's instead of bipolar transistors, the multiplier/divider circuit constructed with bipolar transistors can realize high-linearity compared with those constructed with the MOSFET's. Moreover, the multiplier/divider circuit constructed with bipolar transistors has a very simple circuit structure and is suitable for lowering the supply voltages. To make the delay block operate as a two-quadrant switched-current track & hold circuit, the bias current I_3 is set such that

$$I_3 - {}^{P}A|^{P}X_n| + \sum_{i=1}^{N} R\ ^{i}X_n \geq 0.$$

The current, $I_3 - {}^{P}A|^{P}X_n| + \sum_{i=1}^{N} R\ ^{i}X_n$ $(i \neq p)$, is delayed by one clock in the delay block. In the dumping block, $1 - {}^{P}A|^{P}X_n| + \sum_{i=1}^{N} R\ ^{i}X_n$ $(i \neq p)$, is realized by subtracting the bias current I_4 from the output current of the delay block. The unity constant in $F(^{P}X_n)$ corresponds to $I_3 - I_4$ which is set to 10 μA. The result of this operation is fed back to the input terminal of the operation block. The initial value of the chaotic cell circuit is given by the current source $^{P}X_0$.

When $^{P}A < 1$ and $V_R = 0$, the output of the chaotic cell circuit is given by

$$^{P}X_Q = 1/(1 + {}^{P}A), \quad (3)$$

where $^{P}X_Q$ is an equilibrium point. In the comparator, the chaotic cell circuit is diagnosed from the output of the chaotic cell circuit which is given by Eq.(3). Figure 3 shows the comparator design by using current-mode techniques. The synthesis of the comparator is based on the following equations:

$$^{P}O = \begin{cases} 0, & (\ ^{P}X_Q < I_{th1},\ ^{P}X_Q > I_{th2}\ ) \\ I_u, & (\ I_{th1} \leq {}^{P}X_Q \leq I_{th2}\ ) \end{cases} \quad (4)$$

where I_u is a unit current, I_{th1} and I_{th2} are the threshold currents. From Eqs.(3) and (4), the threshold currents, I_{th1} and I_{th2}, are determined by

$$I_{th1} = 1/(1 + {}^{P}A) - \alpha,$$

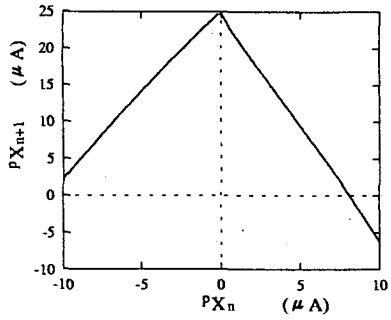

Fig.5 Nonlinear function of the proposed cell circuit.

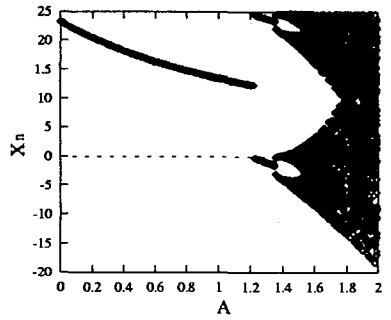

Fig.6 Bifurcation diagram of the proposed cell circuit.

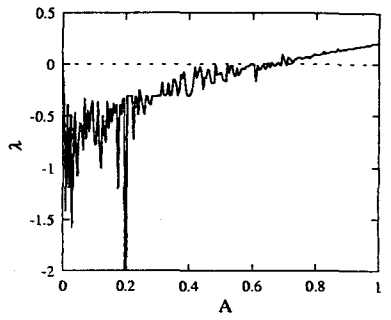

Fig.7 Lyapunov exponent of the bifurcation diagram.

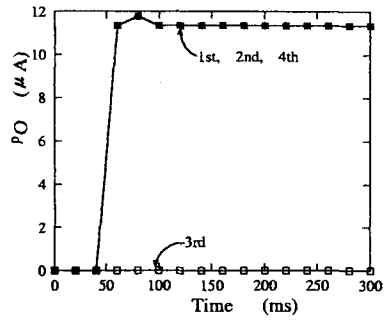

Fig.8 Output waveforms of the comparator.

$$I_{th2} = 1/(1 + {}^{P}A) + \alpha, \quad (5)$$

where α is a constant value. The comparator outputs I_u when the output $^{P}X_Q$ is $I_{th1} \leq {}^{P}X_Q \leq I_{th2}$. On the other hand, the comparator outputs 0 when the output signals $^{P}X_Q$ is $^{P}X_Q < I_{th1}$ or $^{P}X_Q > I_{th2}$. When $^{P}O = 0$, the chaotic cell circuit is considered as the fault cell circuit. In the dumping block, the connection of the chaotic cell circuit with fault can be cut off by setting $V_R = 0$. Hence, the high-dimensional chaos circuit can be constructed with the chaotic cell circuit except the fault cell circuit. In other words, the long working-life of the chaos circuit can be achieved.

3 Simulation

To confirm the validity of the circuit design, SPICE simulations were performed regarding to the circuit shown in Fig.4. The SPICE simulations were performed under the condition that the cell circuit-3 (see in Fig.4) was at fault. In SPICE simulations, the parameters in Fig.2 were set to $V_{dd} = 5V$, $V_b = 2.5V$, $I_2 = 10\mu A$, $I_3 = 30\mu A$, and $I_4 = 20\mu A$.

Figure 5 shows the simulated nonlinear function of the chaotic cell circuit. Figure 6 shows the simulated bifurcation diagram of the chaotic cell circuit. In Fig.6, the existence of chaos can be confirmed using the Lyapunov exponent. The Lyapunov exponent is one of the most famous conditions for generating chaos. The Lyapunov exponent λ for the 1-dimensional chaos circuit is defined as

$$\lambda = \lim_{M\to\infty} \frac{1}{M} \sum_{i=0}^{M-1} \log|\mathbf{DF}(X_i)|, \quad (6)$$

where

$$\mathbf{DF}(X_n) \triangleq \frac{dF(X_n)}{dX_n}.$$

Figure 7 shows the Lyapunov exponent of the bifurcation diagram in Fig.6. Here, $\lambda > 0$ means existence of chaos. In Fig.7, the parameter M in Eq.(6) was set to 10,000. Figure 8 shows the output waveforms of the comparator. In SPICE simulations of Fig.8, the parameters were set to $I_{th1} = 10\mu A$, $I_{th2} = 15\mu A$, and $I_3 = 4\mu A$. As one can see from Fig.8, the cell circuit-3 is at fault. From the simulation results of Fig.8, a 2-dimensional chaos circuit was constructed with the cell circuit-1 and 2.

Figure 9 shows the strange attractors of the 2-dimensional chaos circuit constructed with the cell circuit-1 and 2. The Lyapunov exponent λ for the 2-dimensional chaos circuit is defined as

$$\lambda \triangleq \max\{\lambda(1), \lambda(2) - \lambda(1)\}, \quad (7)$$

where

$$\lambda(1) \triangleq \lim_{M\to\infty} \frac{\log[\|\Pi_{i=1}^{M}[\mathbf{DF}(X_i, Y_i)]\delta\mathbf{L}_i\|/\|\delta\mathbf{L}_i\|]}{M},$$

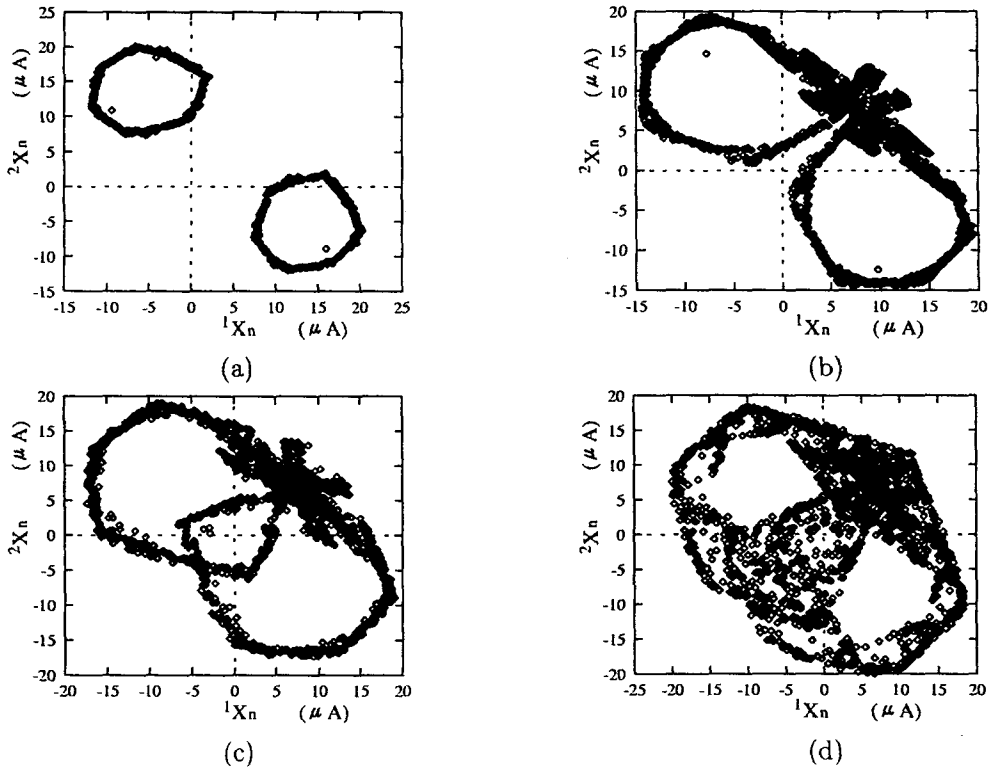

Fig.9 Strange attractors obtained by SPICE simulations. (a) A = $8\mu A$. (b) A = $9\mu A$. (c) A = $10\mu A$. (d) A = $11\mu A$.

$$\lambda(2) \triangleq \lim_{M\to\infty} \sum_{\hat{i}=1}^{M} \frac{\log|\det[\mathbf{DF}(X_{\hat{i}}, Y_{\hat{i}})]|}{M},$$

$$\mathbf{DF}(X_{\hat{i}}, Y_{\hat{i}}) = \begin{pmatrix} \frac{\partial F_1(X_{\hat{i}},Y_{\hat{i}})}{\partial X_{\hat{i}}} & \frac{\partial F_1(X_{\hat{i}},Y_{\hat{i}})}{\partial Y_{\hat{i}}} \\ \frac{\partial F_2(X_{\hat{i}},Y_{\hat{i}})}{\partial X_{\hat{i}}} & \frac{\partial F_2(X_{\hat{i}},Y_{\hat{i}})}{\partial Y_{\hat{i}}} \end{pmatrix},$$

$$\delta \mathbf{L}_{\hat{i}} = \begin{bmatrix} X_{\hat{i}+1} - X_{\hat{i}} \\ Y_{\hat{i}+1} - Y_{\hat{i}} \end{bmatrix}.$$

In the above definitions, $\lambda(1)$ is called the one-dimensional Lyapunov exponent and $\lambda(2)$ is called the two-dimensional Lyapunov exponent. The Lyapunov exponents λ of the strange attractors in Figs.9 (a) $\sim$ (d) were 0.126, 0.096, 0.132, and 0.192, respectively.

4 Conclusion

A discrete-time high-dimensional chaos circuit with array structure has been proposed in this paper. The proposed analog chaos circuit is designed by SI techniques.

The SPICE simulations concerning the proposed circuits designed by SI techniques showed that 1. the proposed circuit can demonstrate various bifurcation modes, 2. the proposed circuit can generate the chaotic signals in spite of fault of the building blocks. This result means that the rate of the acceptable product for chaos IC can be improved. The proposed circuit is integrable by a standard BiCMOS technology.

The theoretical analysis for the bifurcation modes of the proposed circuit is left to the future study.

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