Oscillation Frequency Estimation of Feedback Bridging Faults for Test Circuit Design

Sou Yamamoto, Masaki Hashizume, Hiroyuki Yotsuyanagi, Takeomi Tamesada
Department of Electrical and Electronic Engineering, Faculty of Engineering
The Univ. of Tokushima
2-1 Minamijyousanjima Tokushima-shi, 770-8506 JAPAN
Phone +81-88-656-7473, Fax +81-88-656-7474
E-mail {syama, tume, yanagi4, tamesada}@ee.tokushima-u.ac.jp

Abstract: When a feedback bridging fault is activated, oscillation may be generated in output signal lines. If the oscillation is generated, the fault may not be detected by logic testing. Thus, in the past, we proposed a current sensor to detect feedback bridging faults by supply current testing. The sensor circuit design requires the maximum frequency of oscillation which is generated when feedback bridging fault is excited as a specification. In this paper, an estimation method of the oscillation frequency is proposed. Also, it is shown by some experiments that the frequency obtained by the method can be used for the sensor design.

1. Introduction

It is well known that bridging faults often occur in logic circuits implemented with current technology. The bridging faults are classified into 2 kinds of faults; I/O bridging fault and feedback bridging(FB) faults[1,2].

A bridging fault is activated by providing a logic value and the other one to one of the bridging signal line, respectively. In the case of feedback bridging faults, oscillation of logic value may be generated in the bridging signal lines. If there are odd number of inversions between the bridging signal lines, oscillation of logic value may be generated in the bridging signal lines during the sensitization[1]. If the oscillation is generated, the fault may not be detected by measuring the output logic values.

Bridging faults are easier to be detected by supply current testing than logic testing. In order to detect them by supply current testing, they should be excited but faulty logic value does not always be propagated to primary output signal lines. Also, part of the bridging faults can be detected by logic test method based on stuck-at fault models. Thus, the faults have been tried to be detected by supply current testing.

If a feedback bridging fault does not generate any oscillation, it will be detected with conventional IDDQ sensor circuits like in the case of I/O bridging faults, since extremely large quiescent supply current will continue to flow during the activation. On the other hand, if oscillation of logic value is generated, the supply current will change with time and the fault may not be detected with the conventional sensor circuits. Thus, in the past, we proposed a sensor circuit for detecting feedback bridging faults in combinational circuits, which generate oscillation during the fault activation[3].

Our sensor circuit to detect feedback bridge faults with oscillation is not for measuring the average values of the supply current waveform, but is for measuring high frequency components in the waveform. The frequency depends on oscillation in logic value. Thus, in order to design our sensor, the maximum frequency must be given as a specification.

There can be many bridging faults in a logic circuit. In order to obtain the maximum frequency of the oscillation, we must identify the bridging faults which can generate oscillation. Also, the oscillation frequency of each fault should be estimated. Until now, only one estimation method is proposed in [2]. However, it takes a lot of computational cost to derive the frequency. Since there can be many feedback bridging faults in a circuit, it may be impossible to derive the frequency by the method.

In this paper, an estimation method for the maximum frequency is proposed in section 3 after introducing feedback bridging faults in section 2. By using the method, the frequency is estimated for a CMOS circuit in section 4.

2. FB Faults with Oscillation

A feedback bridging fault is shown in Fig.1. As shown in Fig.1, as for a feedback bridging fault, the logic value of one of the bridging signal lines is effected by the fault propagation generated by the sensitization of the fault.

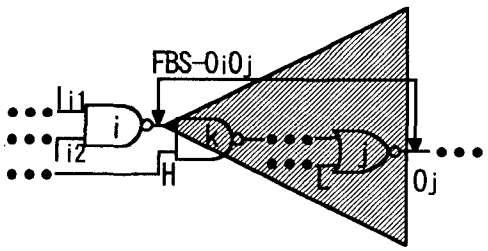


Fig.1 Feedback bridging fault.

When a feedback bridging faults is activated, if oscillation does not occur, large quiescent supply current will flow during the activation. If the oscillation is generated, the supply current will change with time and high frequency components will be generated.

All of the circuits having feedback bridging faults can be modeled as the circuit in Fig.2[4]. An example circuit having a feedback bridging fault is shown in Fig.3. In Fig.3, when PI1=H,PI2=L, the feedback bridging fault FBS-O_AO_B between the signal lines O_A and O_B can be excited. By the excitation, logical oscillation may be generated. Some waveforms generated by the excitation of the feedback bridging fault are shown in Fig.4.

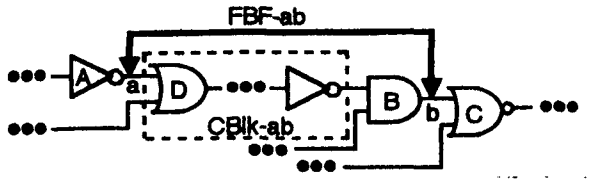


Fig.2 Circuit having FB fault

It depends on the layout design of gates A,B and C and the propagation delay time of the sub-circuit between gates A and B whether oscillation occurs. We proposed in [4] how to identify feedback bridging faults with small computation costs. By using the method, it can be determined whether a feedback bridging fault can generate oscillation.

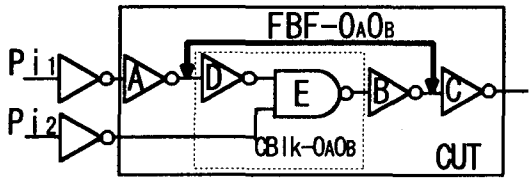


Fig.3 Circuit under test

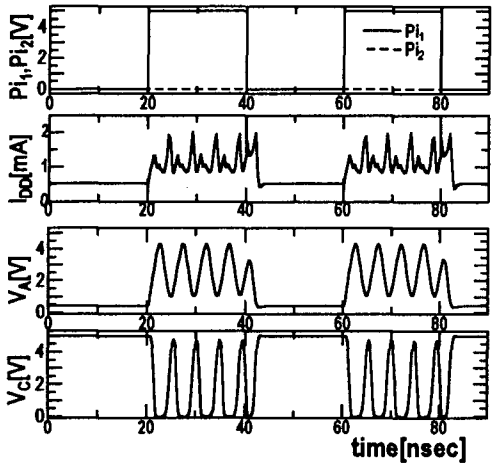


Fig.4 Example waveform of oscillation

3. Our Sensor Circuit for FB faults

Our sensor circuit is shown in Fig.5. As shown in Fig.5, feedback bridging faults are attempted to be detected by using two kind of test circuits in Fig.5; IDD level checker and IDD oscillation checker. IDD level checker is for detecting bridging faults which do not generate oscillation by measuring the quiescent supply current $I_{DDQC}(T_j)$. By using the circuit, it is checked whether Eq.(1) is satisfied.

$$I_{DDQC}(T_j) \square I_{th} \qquad (1)$$

where $I_{DDQC}(T_j)$ is quiescent supply current of the circuit under test(CUT) which is measured with the IDD level checker when an input vector T_j is provided to the CUT and I_{th} is the threshold value for determining whether the circuit is faulty or not.

IDD oscillation checker is for detecting the bridging faults which generate oscillation. Our IDD oscillation checker consists of an I-V transformer, a high frequency amplifier and a demodulation circuit[3]. With the I-V transformer, the supply current(IDD) of the CUT is converted into voltage. An example of output waveform of the IDD oscillation checker is shown in Fig.6. Only the high frequency components in the converted IDD waveform are amplified by the amplifier. The peak value of the amplified waveform is detected by the demodulation circuit. The peak value is used to detect the fault. If Eq.(2) is satisfied, the circuit is determined as faulty.

$$V_{OSC}(T_j) \square V_{OSCth} \qquad (2)$$

where $V_{OSC}(T_j)$ is the output voltage of the IDD oscillation checker obtained when an input vector T_j is provided and V_{OSCth} is the threshold value for determining whether the circuit is faulty or not with the checker. In our test, if one or both of Eq.(1) and Eq.(2) are satisfied, the CUT is determined as faulty.

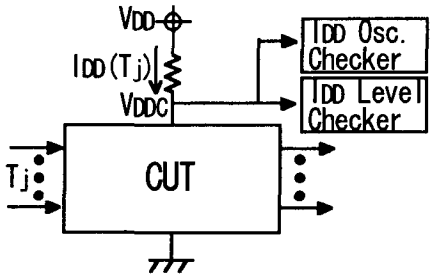


Fig.5 Test circuits for feedback bridging fault

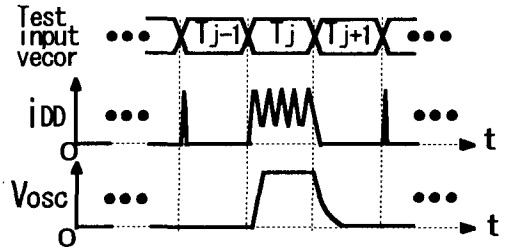


Fig.6 Operation of IDD oscillation checker

As described above, feedback bridging faults are detected by amplifying only high frequency components in the supply current waveform. Thus, in order to design our sensor, the maximum frequency of oscillation must be given as a specification. However, until now, any methods to estimate the frequency have not been proposed.

4. Oscillation Frequency Estimation

In[4], we proposed how to identify feedback bridging

faults with oscillation. In this paper, by using various kinds of characteristic parameters for the identification, oscillation frequency is derived.

V_A waveform in the oscillation in Fig.3 is shown in Fig.7. In [4], the V_A waveform in Fig.7 is modeled as Fig.8 with piece linealized models. The waveform depends on t_r and t_f of V_A obtained from the circuits in Fig.9 and the propagation delays(t_{pdLH} and t_{pdHL}) of CBlk-O_AO_B. Thus, the waveform of V_A is defined with the parameters.

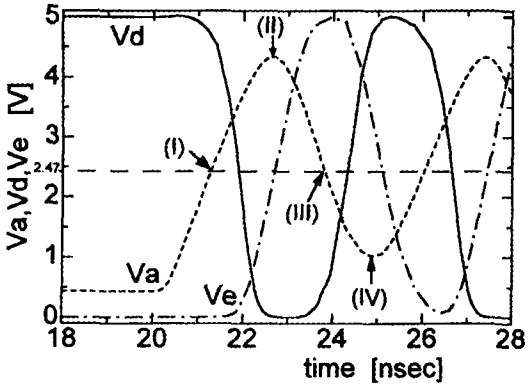


Fig.7 Waveforms in oscillation

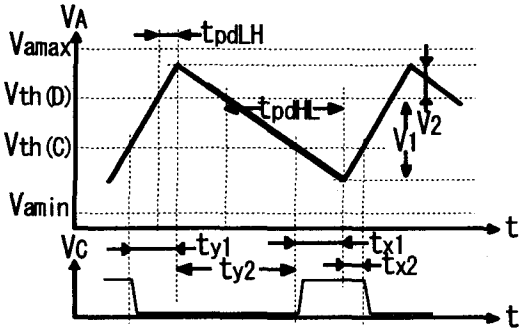
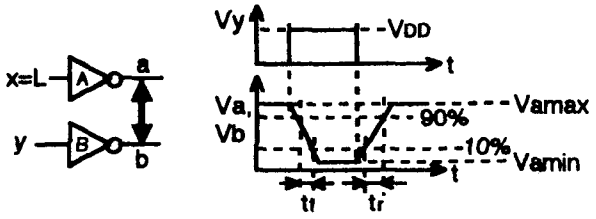


Fig.8 Modeling of circuit operation.

In [4], we proposed three conditions for oscillation. The first one is expressed by Eq.(3). Unless it is satisfied, oscillation will not be generated.

$$V_{amin} < V_{th}(D) \qquad (3)$$

where V_{amin} is the final value of V_a obtained from the experiment in Fig.9(b) and $V_{th}(D)$ is the threshold voltage of gate D in Fig.2.



(a) rise time t_r (b) fall time t_f
Fig.9 Circuit for deriving V_A changes

The second one is expressed by Eq.(4). In order to generate oscillation, V_A should become much smaller than the threshold voltage($V_{th}(C)$) of gate C. If it is not satisfied, the change in V_A can not be propagated to the output of gate C. Therefore, the following condition should be satisfied besides Eq.(3).

$$V_a < V_{th}(C) \qquad (4)$$

The third condition is one in time domain. In order for logical oscillation to appear in the output of gate C, V_A should be smaller than $V_{th}(C)$ until output logical change of gate C can be generated. The condition is specified by Eq.(5).

$$t_{x1} + t_{x2} \square t_r(C) \qquad (5)$$

where $t_r(C)$ is rise time of gate C and t_{x1} and t_{x2} in Fig.8 are defined by Eq.(6) and Eq.(7), respectively.

$$t_{x1} = \frac{V_1 - V_{th}(D) + V_{th}(C)}{V_1} t_{pdLH} \qquad (6)$$

$$t_{x2} = \frac{V_1 - V_{th}(D) + V_{th}(C)}{0.8(V_{amax} - V_{amin})} t_r \qquad (7)$$

In Eq.(6) and Eq.(7), V_1 is used, which is defined in Fig.8.

It is apparent from Fig.8 that the period (T) of the generated oscillation can be obtained by Eq.(8).

$$T = t_{x1} + t_{x2} + t_{y1} + t_{y2} \qquad (8)$$

where t_{y1} and t_{y2} are defined by Eq.(9) and Eq.(10), respectively.

$$t_{y1} = \frac{V_2 + V_{th}(D) - V_{th}(C)}{V_2} t_{pdHL} \qquad (9)$$

$$t_{y2} = \frac{V_2 + V_{th}(D) - V_{th}(C)}{0.8(V_{amax} - V_{amin})} t_f \qquad (10)$$

The oscillation frequency(f) is obtained from Eq.(11).

$$f = 1/T \qquad (11)$$

5. Experimental Evaluation

In order to estimate the frequency of oscillation preciously, circuit simulation should be executed for faulty circuits. However, it takes a large simulation time to obtain the oscillation frequency, since transient analysis must be executed. Furthermore, there are a lot of feedback bridging faults in a circuit. In order to derive the maximum frequency, circuit simulation must be executed for all of the bridging faults. Thus, it is impossible to derive the frequency with circuit simulator.

On the other hand, as described in section 4, the method is based on piece-linearized model of the transient behavior in each logic gate and needs circuit simulation for only small size of circuits in Fig.9. Thus, the maximum frequency can be derived by our method in a practically reasonable time.

In order to examine whether the frequency of oscillation can be derived by our method, the frequency for the circuit in Fig.2 is derived. It depends on the W/L ratios of MOS transistors in gates A and B whether oscillation can occur. Also, the frequency of the oscillation. depends on them. Thus, layouts of the circuits having different W/L ratios in gates A and B are designed with ES2 1.2 μ m CMOS process technology by

using MSK[5]. After that, they are converted into SPICE files, in which permissive capacitors between gates are included. The obtained SPICE files are simulated with PSPICE. From the simulation results, the frequency of oscillation f_0 is obtained and is compared to the one obtained by our method. The results are shown in Table 1. In Table 1, error rate (Er), which is defined by Eq.(12), is calculated for the comparison.

$$Er = \frac{f_0 - f}{f_0} \times 100 \qquad (12)$$

Table 1 Experimental results

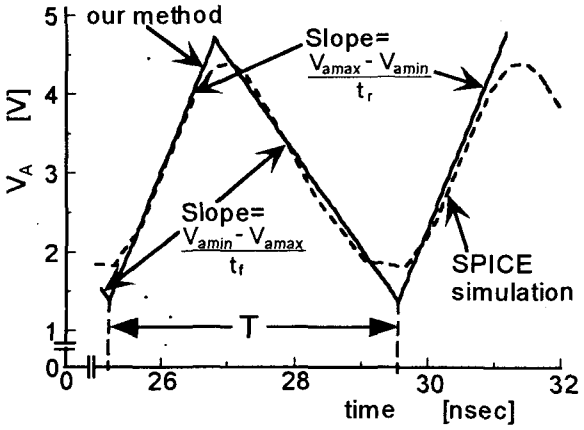
W/L ratio				Osc. Freq. [MHz]		error rate
gate A		gate B		Spice	our	[%]
pMOS	nMOS	pMOS	nMOS	Sim.	method	
13/1	5/1	5/1	5/1	234.51	279.67	19.26
10/1	〃	〃	〃	226.98	229.78	1.23
5/1	〃	〃	〃	212.44	174.26	-17.97
7/4	〃	〃	〃	189.62	140.08	-26.13
3/2	〃	〃	〃	187.86	137.18	-26.98

As shown in Table 1, our estimation method can generate large error. The results of comparison with the waveforms obtained by SPICE simulation are shown in Fig.10. As shown in Fig.10(b), the error stems that our method can not detect that Va becomes larger than the VDD voltage. However, in the case of the faults which can generate the maximum frequency, Va can not be beyond the VDD voltage. Thus, the maximum frequency will be derived by our method. In fact, the maximum frequency obtained by SPICE simulation is 234.51MHz. The maximum frequency obtained by our method is 279.67MHz. It means that by using IDD oscillate checker designed with our derived frequency, all feedback bridging faults with oscillation can be detected.

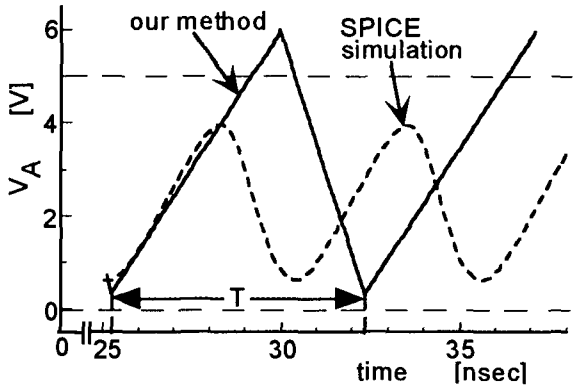
6. Conclusion

In this paper, an estimation method of the maximum frequency of oscillation, which is generated by feedback bridging faults, is proposed. The frequency is necessary to design our supply current sensor for detecting feedback bridging faults in logic circuits. The method is evaluated by some experiments. The experimental results shows that by designing the sensor to detect feedback bridging faults which can generate oscillation of the maximum frequency, all of the feedback bridging faults can be detected.

Our method is based on piece-linearized models. Thus, the frequency can be derived with small computational cost. Since there are a lot of feedback bridge faults in a large size of circuit, it is expected that our method is very effective for estimating the maximum frequency of oscillation.



(a) W/L=10/1



(b) W/L=7/4

Fig.10 Comparison with Spice simulation.
(W/L ratio of PMOS in gate A is changed.)

References

[1]S.Xu and S.Y.H.Su, "Detecting I/O and Internal Feedback Bridging Faults," IEEE Trans. on Computers, pp.553-557(1985)

[2]Y.K.Malaiya and A.P.Jayasumana and R.Rajsuman, "A Detailed Examination of Bridging 81(1986).

[3]M.Hashizume et.al: "A Current Sensing Circuit for Feedback Bridging Faults", proc. of IEEE International Workshop on IDDQ Testing, pp.110-113(1997)

[4]M.Hashizume et.all: "Identification of Feedback Bridging Faults with Oscillation", proc. of the IEEE Ninth Asian Test Symposium, pp.25-30(1999).

[5]E.Sicard : Introduction to microelectronics Version 5.1, INSA Electronic Engineering School at the University of Toulouse(1995).