Circuit Design of a Ternary Flip-Flop Using Ternary Logic Gates

Jong-Heon Kim*, Jong-Hak Hwang*, Seung-Yong Park*, Heung-Soo Kim*
*Circuit & System Lab. Dept. of Electronic Eng. Inha University. KOREA
253 Yonghyun-Dong, Nam-Gu, Inchon, South Korea, 402-751
Tel: +82-32-860-7413
Fax: +82-32-868-3654
E-mail: g1991173@inhavision.inha.ac.kr

Abstract: We present the design of ternary flip-flop which is based on ternary logic so as to process ternary data. These flip-flops are fabricated with ternary voltage mode NOR, NAND, INVERTER gates. These logic gate circuits are designed using CMOS and obtained the characteristics of a lower voltage, a lower power consumption as compared to other gates. These circuits have been simulated with the electrical parameters of a standard 0.25 micron CMOS technology and 2.5 volts supply voltage. The Architecture of porposed ternary flip-flop is highly modular and well suited for VLSI implementation, only using ternary gates.

1. Introduction

In recent years, the research on multiple-valued logic(MVL) has attracted attention of logic designers because it can increase the information density of circuits, and thus leading to the reduction of the number of connections and pins, and the saving of on-chip area of IC[1,2]. However, it also leads to the complexity in designing and analyzing circuits along with the increase of the number of signal levels. Among the various types of MVL, the ternary logic is one of the most popular logic because of the simpler circuit implementations and lower interconnection cost estimations[1].

Several static and dynamic ternary logic circuits have been proposed. The circuit realization of MVL gates using I^2L, charge–coupled divices, voltage-mode CMOS, current-mode CMOS technologies was reported in the literature[3]-[9]. These circuits are generally multiple-powered circuits and they require complex processing to fabricate both depletion and enhancement CMOS transistors[10] or multithreshold transistors[11]. Complex multiphase clocking scheme may also be required in the case of dynamic circuits[12].

In this paper a new voltage-mode CMOS ternary logic circuit and a ternary flip-flop design method using these are presented. It thus minimizes spikes and offers low power supply noise advantages over other implementations. The circuit may be useful in mixed-mode integrated circuits whose performance accuracy is limited by the effects of the digital switching noise generated by the digital circuits. In addition, the proposed circuits require a single power supply.

The circuit descriptions of the basic gates(INVERTER, NAND, NOR) are presented and their static and dynamic performance characteristics have been investigated using HSPICE simulations.

There are three logic values(0,1,2) for signals in this circuits. So, When analyzing ternary circuits, we must consider the response to six transition of input signals between three vlotage levels as well as the response of circuits to three values of input signals.

2. Basic Operations to Present MVL Function

The operations of conjunction and disjunction are used for implementation of multiple-valued logic function[13]. We define the conjunction and disjunction for two variables, x, y $\in$ {0,1,2,·····,P-1}

AND operation $x \wedge y = MIN(x,y)$
OR operation $x \vee y = MAX(x,y)$
INVERTER operation $x' = (N-1) - x$

Where, conjunction MIN(x,y) is the minimum value of variables, x,y and disjunction MAX(x,y) is the maximum value of variables, x, y. x' is the complement of x, N means the radix of this circuit.

3. Design of Ternary Flip-Flop

3.1 The Design of Ternary Basic Flip-Flop(TFF)

TFF circuit can be constructed from two Ternary NAND(T-NAND) gates or two Ternary NOR(T-NOR) gates. These constructions are shown in the logic daigrams of Fig.1 and characteristic table for the basic TFF is in Table.1. It defines the logical property of the flip-flop. The circuit forms a basic flip-flop upon which other more complicated types can be built. The cross-coupled connection from the output of one gate to the input of the other gate constitutes a feedback path. For this reason, the circuits are classified as the asynchronous sequential circuits. The input is defined as a set which consists of distinct elements 0, 1 and 2 (0v, 1.25v, 2.5v).

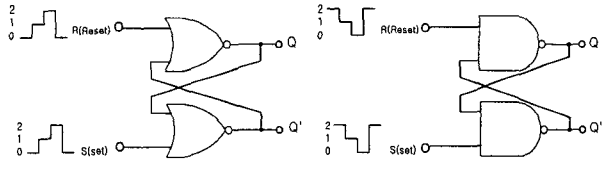


Fig.1 Logic Diagram of basic TFF Circuit

Table.1 Characteristic Table

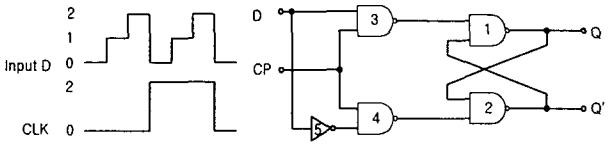
R	0	0	0	1	1	1	2	2	2
S	0	1	2	0	1	2	0	1	2
Q(t+1)	Q(t)	2, if Q(t)=2 1,otherwise	2	0, if Q(t)=0 1,otherwise	1	1	0	0	0

3.2 The Design of Ternary D Flip-Flop(TDFF)

The TDFF shown in Fig.2(b) is the modification of the ternary basic flip-flop. NAND gates 1 and 2 form a basic flip-flop and gates 3, 4 and 5 connected with that, form the TDFF. To analyze the operating characteristic of the TDFF of Fig.2, we must remember that the output of a ternary NAND gate is always 2 if any input is 0, and the output is 0 when both of two inputs are 2. When each of inputs is 1 and 1, 1 and 2, 2 and 1, the output is 1.

We define that when the clock is a high-level signal, the logical value of the clock is 2, and if the clock is a low-level signal, that of the clock is 0. The value of Input D goes directly to the S input, and its complement, through gate 5, is applied to the R input.

Exam 1) As a starting point, assume that the D input is 0 and the clock is high, and changes Q(t) to 0, to 1, and to 2, so that output Q(t+1) is always 0, that is, D. In the same manner, it is possible to show that the characteristic of the TDFF of table 2. The operating characteristic of the TDFF according to the change of input D and clock is shown in table 2.



(a) Input and Clock (b) Logic diagram with T-NAND gates and T-INVERTER gate

Fig.2 Clocked Ternary D Flip-Flop

Table.2 Truth table of the TDFF

Input	D	0	0	1	1	2	2
	Clk	0	2	0	2	0	2
Q(t)	0	0	0	0	1	0	2
	1	1	0	1	1	1	2
	2	2	0	2	1	2	2

(a) Operation table

D	Q(t)	Q(t+1)
0	*	0(D)
1	*	1(D)
2	*	2(D)

(b) Characteristic table

3.3 The Design of Ternary T Flip-Flop(TTFF)

The TTFF shown in Fig.3. NOR gates 1 and 2 form a basic flip-flop and gates 3 and 4 connected with that, form the TTFF. In order to analyze the operating characteristic of the TTFF of Fig.3, we must know that the output of a ternary NOR gate is always 0 if any input is 2, and the output is 0 when both of two inputs are 0. In case of the values of two inputs are 0 and 1, 1 and 1, 1 and 0, the output is 1.

The value of Input T goes directly to the S input and R input, through gate 3 and 4, at the same time.

Exam 2) To begin with, assumming that the T input is 0 and the clock is high, and changes Q(t) to 0, to 1, and to 2, output Q(t+1) is always 0, 1, 2 in order, that is, Q(t). In the same manner it is possible to show that the characteristic of the TTFF of table.3. The operating characteristic of the TTFF according to the change of input T and clock is shown in table.3.

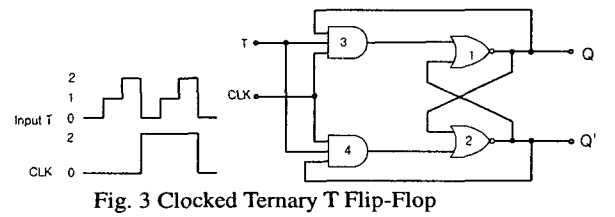


Fig. 3 Clocked Ternary T Flip-Flop

Table.3 Truth table of the TTFF

Input	T	0	0	1	1	2	2
	Clk	0	2	0	2	0	2
Q(t)	0	0	0	0	0	1	0	2
	1	1	1	1	1	1	1	1
	2	2	2	2	1	2	0

(a) Operation table

T	Q(t)	Q(t+1)
0	*	Q(t)
1	*	T
2	*	Q(t)'

(b) Characteristic table

3.4 The Design of Ternary JK Flip-Flop(TJKFF)

The TJKFF shown in Fig.4 is the extension of the ternary basic flip-flop. NOR gates 1 and 2 form a basic flip-flop and gates 3 and 4 connected with that, form the TJKFF. To analyze the operating characteristic of the TJKFF of Fig.4, the output of a ternary AND gate is always 0 if any input is 0, and the output is 2 when both of two inputs are 2. When each of inputs is 1 and 1, 1 and 2, 2 and 1, the output is 1, that is to say, that of a ternary AND gate is obtained by the operation of conjunction, MIN(x,y)

The input J and K behave like inputs S and R to set and clear the flip-flop(note that in a JK flip-flop, the letter J is for set and the letter K is for clear).

Example, in the first place, assumming that the present output Q(t) is 0 and the clock is high, and changes each of the input J and the K to 0, to 1, and to 2, the next output Q(t+1) depends entirely on the input J, having no connection with the input K. In the same manner, if the Q(t) is 1, it depends on the Q(t), unconcerned with the input J and the input K. When Q(t) is 2, the output Q(t+1) counts on the the complement of the input K, except the input J.

In this method, the operating characteristic of the TJKFF according to the change of the input J, the input K and the clock is shown in table.4.

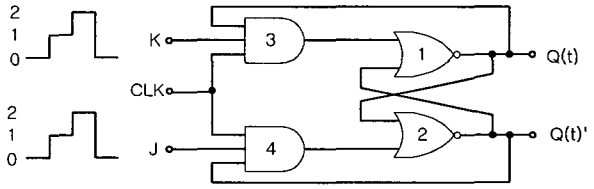


Fig.4 Clocked Ternary JK Flip-Flop

Table.4 Truth table of the TJKFF

Input	J	0	0	0	1	1	1	2	2	2
	K	0	1	2	0	1	2	0	1	2
Q(t)	0	0	0	0	1	1	1	2	2	2
	1	1	1	1	1	1	1	1	1	1
	2	2	1	0	2	1	0	2	1	0

(a) Operation table

Q(t)	0	0	0	1	2	2	2
J	0	1	2	*	*		
K	*			*	0	1	2
Q(t+1)	J			1 (Q(t))	K'		

(b) Characteristic table

3. Design of Ternary basic gates

3.1 The Design of Ternary INVERTER gate

The circuit of the ternary INVERTER gate using voltage-mode CMOS logic circuits is shown in Fig.5. It is designed by NMOS and PMOS, like as original binary

INVERTER. The output inverting each input is obtained by using the complement operation.

The power supply voltage is 2.5v, Each of the input signals(or output signals) is 0v, 1.25v, 2.5v. And the logical values 0, 1 and 2 correspond to 0V, 1.25V, 2.5V. The operating characteristic of the ternary INVERTER circuit is shown in table.5 and its HSPICE simulation results are shown in Fig.6. Note that the M1 and M2 form an ordinary INVERTER.

Table.5 Characteristic table ternary INVERTER gate

IN	OUT
0	2
1	1
2	0

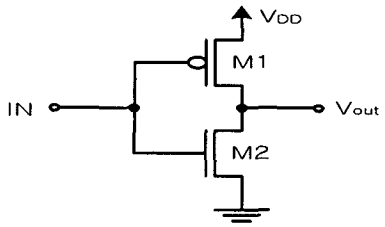


Fig.5 The design of ternary INVERTER circuit

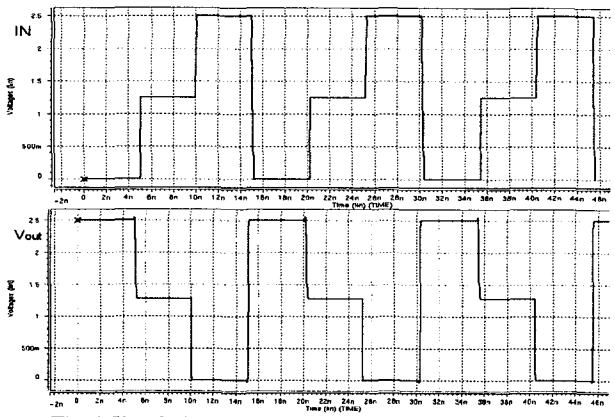


Fig.6 Simulation result of ternary INVERTER circuit

3.2 The Design of Ternary NAND gate

The circuit of the ternary NAND gate using voltage-mode CMOS logic circuits is shown in Fig.7. Note that the M1~M4 form an ordinary NAND and M5 ~ M8 form switching circuit. When IN1 and IN2 have the logical value of 1 or 2, higher than threshhold voltage, M5 and M6 operate normally. And M5 and M6 generate 1.25V by the regulation of transistor size properly. Therefore, in case that IN1 and IN2 have the logical values of 1 and 1, 1 and 2, 2 and 1, the output voltage V_{out} is 1(1.25V). Transister M7 and M8 operate if any inputs is a logical value 0(0V) and the output voltage is 2(2.5V). The operating characteristic of the ternary NAND circuit is shown in table.6 and its HSPICE simulation results are shown in Fig.8.

Table.6 Characteristic table ternary NAND gate

	0	1	2
0	2	2	2
1	2	1	1
2	2	1	0

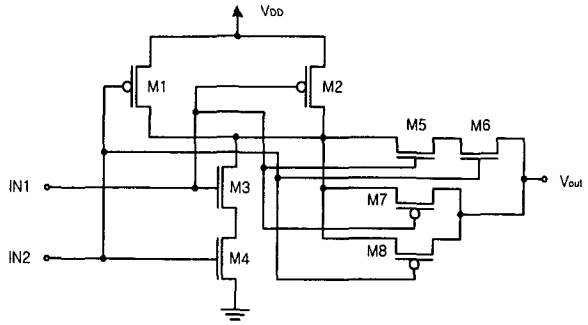


Fig.7 The design of ternary NAND circuit

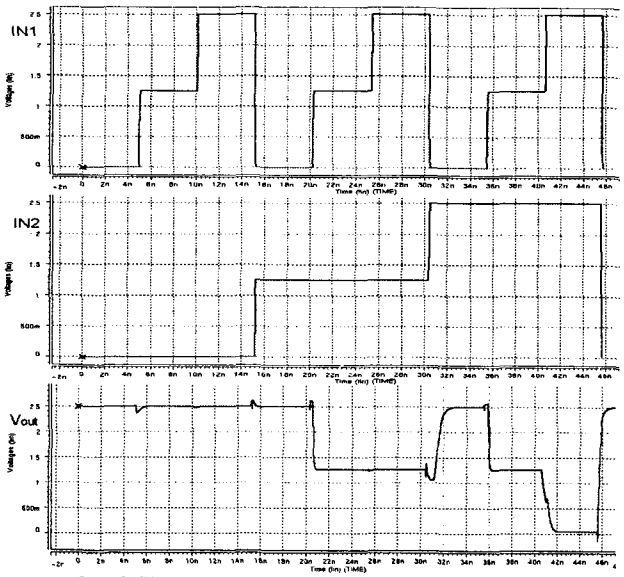


Fig.8 Simulation result of ternary NAND circuit

3.3 The Design of Ternary NOR gate

The circuit of the ternary NOR gate using voltage-mode CMOS logic circuits is shown in Fig.9. Note that the M1~M4 form an ordinary NOR and M5 ~ M8 form switching circuit. When the input IN1 and IN2 have the value of 0 or 1, lower than threshhold voltage, PMOS transistors M5 and M6 operate normally. PMOS transistor M1 and M2 operate in the logical value of 1 like doing in that of 0 with increasing the size of transistor. Therefore, when each of input IN1 and IN2 is 00, 01, 10, 11, the circuit formed with M1~M4 generate output, 2(2.5V). On the other hand, when IN1 and IN2 are only the logical values 0 and 0, the M5 and M6 operate and generate output voltage 2.5V. Transister M7 and M8 operate if the value of any input is a logical value 1(1.25V), transister M7 and M8 operate. And the Vout is 1(1.25V) by the regulation of transistor size properly. Of course, M7 and M8 operate, the value of any input is 2(2.5V) but the value of output of the M1~M4 is 0. Therefore, the output voltage(Vout) is 0.

The operating characteristic of the ternary NOR circuit is shown in table.7 and its HSPICE simulation results are shown in Fig.10.

Table.7 Characteristic table ternary NAND gate

	0	1	2
0	2	1	0
1	1	1	0
2	0	0	0

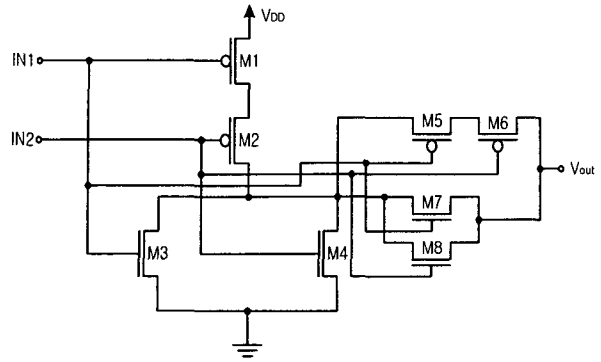


Fig.9 The design of ternary NOR circuit

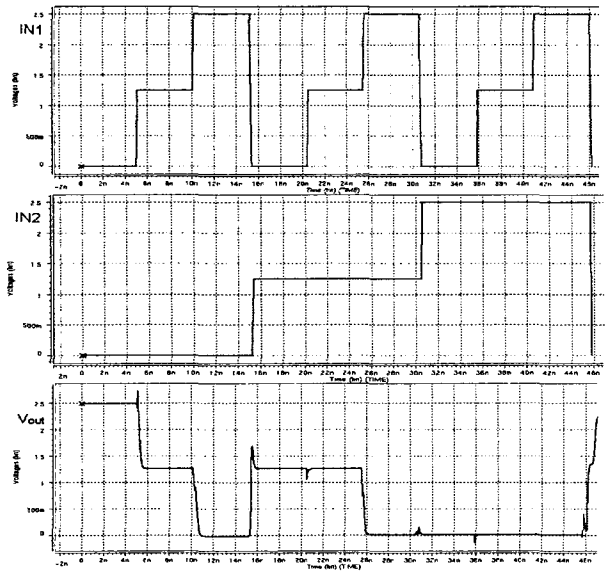


Fig.10 Simulation result of ternary NOR circuit

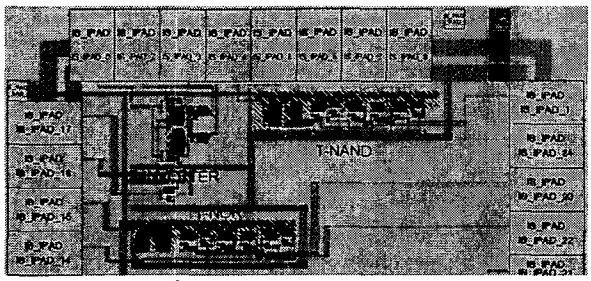


Fig.11 Layout of the ternary logic gates

4. Conclusion

In this paper, the switched voltage CMOS ternary logic gates and the ternary flip-flops using that logic gates have been described. The performance characteristics of the logic gates are investigated by using HSPICE simulations. The obtained results indicate that the proposed circuits exhibit good noise margin of about 15% of the power supply voltage and propagation delay times of less than 1ns in most case. The propagation delay can be improved by increasing the supply voltage and the aspect ratios of the transistors used, at the expense of increased power consumption. This circuits have advantages in the point of view : ①Less interconnections, ②Operate at the lower supply voltage, ③Less power consumption(about 1μw). Results for deep submicron technologies(0.25μm) show the effects of the method for future multiple-valued processes. Also, the proposed ternary flip-flops were presented by a new and an efficient circuit design methodology. Namely, this flip-flops can be more easliy implemented in the gate level than in the MOSFET level.

The implementation of the flip-flop circuits and the remove of the glitch in the gate circuits will be the next theme of this paper.

References

[1]Hurst, S.L., "Multiple-valued logic - Its status and its future," IEEE Trans. On Computer, C-22, pp.1160-1179, 1984

[2]Butler, S.W., J.T., "Profiles of topics and others of the International Symposium on multiple valued logic for 1971-1991," Proceeding of 22nd IEEE Int. Symp. On multiple valued logic, Sendai, pp.372-379, 1992

[3]Yasunori Nagata., "Design of an Asynchronous Digital System with B-ternary Logic," in Proc. 27th ISMVL, pp.256-271, May. 1997.

[4]A. H. M. SHOUSHA., "Switched-current CMOS ternary logic circuits," INT. J. ELECTRONICS, vol. 79, No. 5, pp.617-625, 1995.

[5]A. Jain, R.Bolton, and M. Abd-El-Barr, "CMOS multiple-valued logic design Part I : Circuit implementation," IEEE Trans. Circuit Syst., vol.40, pp.503-514, Aug. 1993.

[6]A. Jain, R.Bolton, and M. Abd-El-Barr, "CMOS multiple-valued logic design Part II : Function realization," IEEE Trans. Circuit Syst., vol.40, pp.515-522, Aug. 1993.

[7]Y.J. Chang and C.L.Lee, "Synthesis ofmulti-variable MVL functions using hybrid mode CMOS logic," in Proc. 24th ISMVL, pp.35-41, May. 1994.

[8]K.W. Current, "Multiple valued logic:Curren-mode CMOS circuits," in Proc. 23th ISMVL, pp.176-181, May. 1993.

[9]C.Y. Wu and H.Y Hauang, "Design and application pipelined dynamic CMOS ternary logic and sample ternary differential logic," IEEE J. Solid-State Circuit, vol. 28, pp. 895-906, Aug. 1993.

[10]Balla, P.C., and Antoniou, A., "Low power dissipation MOS ternary logic family", IEEE Journal of Solid-state Circuits, 19, pp.739-749, 1984

[11]Wu, X.W., Prosser, F.P., "CMOS ternary logic circuits". Proceedings of the Institution of Electrical Engineers, PtG. 137, pp.21-27, 1990.

[12]Wu, C.Y., and Huang, H.Y., "Design and application of pipelined dynamic CMOS ternary logic and simple ternary differential logic, IEEE Journal of Solid-state Circuits, 28, pp.895-906, 1993.

[13]M. Davio and J. P. Eeschamp, "Synthesis of discrete functions using I^2L technology," IEEE Trans., Comput., vol. C-30, pp.653-661, sept. 1981.