DRAM의 Refresh 시간 개선을 위한 불순물 농도 최적화에 관한 연구

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The Study on Impurity Concentration Optimizing for the Refresh Time Improvement of DRAM

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Abstract

The control of the data retention time is a main issue for realizing future high density dynamic random access memory.

In this paper, we propose the new implantation scheme by gate-related ion beam shadowing effect and buffer-enhanced Δ Rp increase using buffered N- implantation with tilt and 4X-rotation that is designed on the basis of the local-field-enhancement model of the tail component. We report an excellent tail improvement of the retention time distribution attributed to the reduction of electric field across the cell junction due to the redistribution of N- concentration which is intentionally caused by Ion Beam Shadowing and Buffering Effect using tilt implantation with 4X-rotation.

I. Introduction.

Improvement of the refresh time distribution is a key problem for realizing future high density DRAM because the required refresh time doubles with each successive generation. There are several leakage current mechanisms in which the stored data disappears. The mechanisms of data disappear is as follow, 1) Junction leakage current between the junction, 2) Junction leakage current from the capacitor node contact, 3) Subthreshold leakage current if the transfer transistor, 4) Capacitor dielectric leakage current, 5) Gate induced drain leakage current at the capacitor node, and 6) Gate insulator leakage current.(Fig.1-1) The novel junction process scheme in DRAM cell with STI has been investigated to improve the tail component of DRAM refresh time distribution. In this paper, we propose buffered N- implantation with angle and rotation process scheme that is designed on the basis of the local field-enhancement model of the tail component[1] and report an excellent improvement effect in tail distribution of refresh time without device degradation. The STI combined with CMP process has become the most promising isolation scheme for 0.18um and beyond[2]. However, the refresh time of DRAM cell decreases by the increased cell junction leakage current that is caused by STI dislocation[3] and the large electric field effect of cell storage junction[4].

It has been reported that the increase of electric field across the cell junction enhances thermionic field emission current from storage node and forms the poor tail distribution of refresh
time[5].

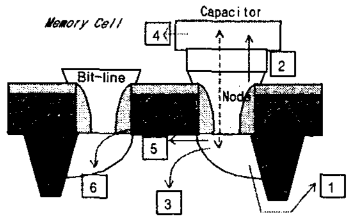

Fig.1-1. Cell leakage current mechanism.

In this paper, we propose a novel method of optimizing the impurity concentration in N- junction region to reduce the local field-enhanced thermionic field emission current, resulting in an excellent tail distribution of refresh time without trade-offs of cell transistor threshold voltage and operation current.

The fabricated device has W / L = 15 / 0.26㎛ NMOSFET, 0.18㎛ cell, shallow trench isolation (depth=350nm), 7.0nm wet and/or nitride gate oxide, FG light doped drain silicon nitride sidewall.

II. Fabrications

N- implantation with/without buffer layer and tilt-rotation, several experiments with different process provided in Table1[Conventional / Buffer / Buffer+Ion]. Then 65nm Si_3N_4 sidewall spacer was formed and then deep source /drain implantation(As) was carried out. The final process was RTA annealing at 1000℃ for 10seconds(to activate arsenic ions). For each splitting condition, we simulated and measured the junction characteristics to analysis Buffer oxide and nitride layer was deposited and etched the field area for active area definition. Shallow trench etching was performed after thin nitride layer was etched. Filling the trench gap with high density plasma oxide, and densification at high temperature, then CMP was carried out for planarization. Nitride and pad oxide were removed by wet etching. Channel ion implantation performed to control threshold voltage after high density plasma densification. The fabrication process of MOSFETs was based on L=0.26um with 7.0nm wet annealed oxide. The gate electrode was patterned by the KrF lithography. In order to verify that the refresh time distribution of DRAM cell and STI is dependent on the retention time.

(Table 1) Process split Condition

Process	Implantasion Condition	Angle	4-rotations	Buffer
[redacted]	P.20Kev, 2.0E13/cm²	X	X	X
	P,40Kev, 2.0E13/cm²	X	X	O
	P,40Kev, 2.0E13/cm²	O	O	O

III. Simulation

For the comparison of junction profile after full process and concentration profile just after N- implantation, process simulation corresponding to each splitting condition was performed. At the bias condition of fully charged state, the variation of electric field across the junction according to each process scheme was modeled using MEDICI simulator.

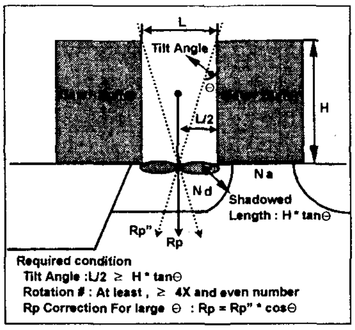

Fig.3-1. Schematic representation of the least requirements of the new process scheme.

Nd/Na ratio in the surface region of the storage node junction. First, it is necessary to meet the tilt angle and rotation number for avoiding the local N- concentration loss in self aligned implantation region due to the overshadowing between the This scheme is composed of the 200Å deposited SiO2 layer and small angle-tilted implantation with 4X[4 times]-rotation. The implantation with buffer layer makes it possible to increase implanting energy, resulting in larger ΔRp at the same Rp (projected range) compared to that without buffer layer, which enables to obtain the broadened distribution of N- concentration along the vertical length. In addition, the small angle-tilted implantation with 4X-rotation produces the local reduction of impurity concentration due to the gate-related ion beam shadowing effect. Even though the encroached region as well as the shadowed region forms alternately at the gate edge into the deeper junction during the ion beam scanning, it may not influence the electric field. Furthermore, the increase of effective channel length due to the extended implant-masking area by buffer layer and the shadowed region by tilt implantation with rotation provides the feasibility of practical cell transistor without enhancing short channel effect. Especially, the adoption of this new implantation scheme in a real product is limited by several process factors such as tilt angle, number of rotation and neighboring gates as shown in Fig.3-1. If 2X rotation is applied, the local loss of N- concentration due to the overshadowing gets worse and results in the increase of N- sheet resistance. To solve this problem, the tilt angle is limited so that the shadowed region caused by tilt implantation should not exceed the half of gate-gate space as given by equation (1). And the number of rotation should be required to be even number and at least 4X.

$$L / 2 \geq H * \tan\theta \qquad (1)$$

represents tilt angle. And also, in case of larger tilt angle, the variation of Rp should be compensated according to equation (2).

$$Rp = Rp * \cos\theta \qquad (2)$$

Second, Nd/Na ratio becomes the limiting factor because this new scheme is based on the local electric field reduction by the control of the impurity concentration in N- junction. Generally, Na is considered in view point of reducing the fluctuation of threshold voltage(Vth) in order to suppress the leakage current in off state of cell transistor. However, the excessive increase of Na results in lowering the degree of freedom of this new implantation scheme for tail component improvement of the retention time distribution. Thus, it is important to choose the smallest Na to maintain Vth of cell transistor without degrading device As a result of simulation, electric field contour plot for the splitting is shown in Fig.3-2. The values of maximum electric field were observed, 0.396MV/cm for Conventional process scheme, 0.358MV/cm for Buffer and 0.343 MV/cm for Buffer+Ion, respectively. characteristics.

In Fig.3-3, the observed electric field distribution along the horizontal length represents the strong feasibility of buffer+Ion process scheme. Buffer+Ion process scheme allows for the superior junction leakge characteristics as shown in Fig.3-4. In Fig.3-5, we also observed 110% improvement effect of Tref@1E-4%(the refresh value which is corresponding to 1E-4% failure bit in the cumulative probability plot) for the DRAM cell with Buffer process scheme and 170% with Buffer+Ion compared to Conventional, respectively. This indicates that both of the factors, such as implantation with buffer layer and tilt / 4directions-rotation, have a large contribution of tail distribution influencing independently. Measured Tref@1E-4% values for each splitting condition were in an excellent agreement with electric field model.

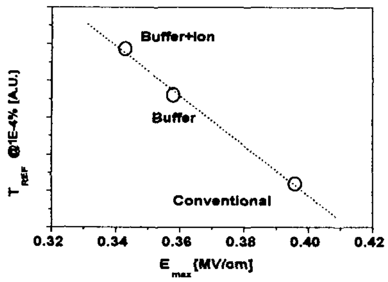

Fig.3-2. Simulated of Electric Field across the junction depletion region according to N- implantation process schemes.

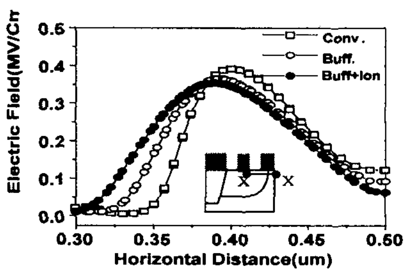

Fig.3-3. Electric field distribution along the horizontal length.

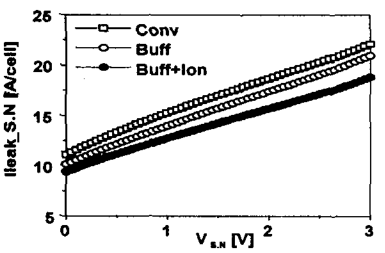

Fig.3-4.Measured junction leakage from storage node for each splitting condition.

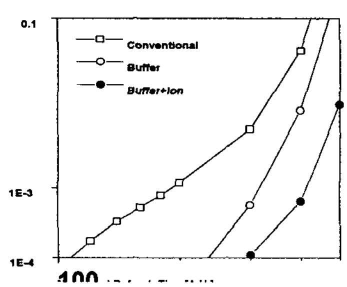

Fig.3-5. Cumulative probability plot of measured refresh time.

IV. Conclusion

We showed that Buffer+Ion process scheme had an excellent refresh time tail distribution without trade-offs of threshold voltage and operation current. And , the observed results were in an excellent agreement with the local field-enhancement model of the tail component. The improvement in tail distribution of refresh time is attributed to the reduction of maximum electric field across the junction depletion region due to the redistribution of N- concentration that is intentionally caused by buffered and tilted implantation with 4directions -rotation.

References

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