A Current-mode peak detector circuit

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Abstract

In this article, a current mode peak detector circuit is presented. The simple circuit configuration comprises four MOS transistors and one external capacitor. The realization method is suitable for fabrication using CMOS technology and all transistors are operated in their saturation region. The proposed circuit exhibits a very low drop rate and provides high accuracy, high-speed and wide dynamic range. The proposed circuit has very low power dissipation and operates using a single 2.5V supply. Simulation results confirmed the characteristic of the proposed circuit are also included.

1. Introduction

A peak detector is a useful circuit building block used in electronic systems, analog measurement and instrumentation. For example, it can be used in AC voltmeter to measure non-sinusoidal waveform [1], [2], an automatic voltage regulation loop of an uninterruptible power supply [3], a nuclear pulse spectroscopy [4], an automatic voltage gain control in radio receiver [5] and a floppy and hard disk drives [6]. Classical approach that can usually be employed to realize peak detector is through the use of diode and capacitor. The limitation of this approach is the detecting signal amplitude must greater than the diode "on" voltage to avoid an inaccuracy. Usually, the application of peak detector requires the signal amplitude in the order of millivolts or microampere. The use of diode in the feedback loop of an operational amplifier (op-amp) has been used to improve an accuracy of the classical approach. However, in practice it is not economical for integrated circuit design, particularly for the case of op-amp type, since each op-amp requires a substantial chip area in itself. Recently, the high frequency peak detector realizable in monolithic form is introduced [5]. The realization technique is based on bipolar technology and provides a differential output to eliminate the output offset voltage. In CMOS technology, the further references on the realization of a peak detector can be found in [6] - [8]. The MOS precision current peak detector is proposed in [6]. The advantage of this approach is a simple circuit configuration and a low voltage operation. However, the use of MOS transistors operate in class B and MOS diode are effected the speed of the peak detector. The purpose of this article is to propose a CMOS circuit technique for the realization of a current peak detector. The realization method can result in fully integrated peak detector. The resulting performances of the circuit have high accuracy, high speed and wide dynamic range.

2. Circuit description

The proposed current-mode CMOS peak detector is shown in figure 1. Assuming that the transistors M_1 and M_2 are well matched and all transistors operate in their saturation regions. The operation of the circuit can be explained as follows. The transistors M_1 - M_3 form as a unity gain current mirror. The transistors M_3 and M_4 function as a current follower to provided a charge current to the capacitor C_1 and a path of the negative current I_{in}, respectively. If the positive input signal current $I_{in} > 0$, the current I_{in} flows through the input of the current mirror $M_1 - M_3$ that cause the voltage at node A to increase and the gate-source voltage of the transistor M_4 to decrease effecting the transistor M_4 to cutoff. The gate-source voltage of the transistor M_1, V_C, is risen and held by the capacitor C_1 with the charge current from the transistor M_3. The voltage V_C can be written as

$$V_C = \sqrt{\frac{2I_{in}}{\beta_1}} + V_T \qquad (1)$$

where β_1 and V_T are the transconductance parameter ($K'_P W/L$) and the threshold voltage, respectively, of the transistor M_1. The gate-source of the transistor M_2 is connected to the capacitor C_1 then the drain current of the transistor M_2, I_{out}, can be stated as

$$I_{out} = I_{d1} = K'_P \frac{W}{2L}(V_C - V_T)^2 \qquad (2)$$

where I_{d1} is the drain current of the transistor M_1. When the capacitor voltage rises to the steady voltage V_C that causes the transistor M_3 to cutoff. The voltage V_C still forces the transistors M_1 and M_2 to operate equal drain current. If the