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Fabrication of interface-controlled Josephson junctions using Sr_2AlTaO_6 insulating layers

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Abstract

We fabricated ramp-edge Josephson junctions with barriers formed by interface treatments instead of epitaxially grown barrier layers. A low-dielectric Sr_2AlTaO_6(SAT) layer was used as an ion-milling mask as well as an insulating layer for the ramp-edge junctions. An ion-milled $YBa_2Cu_3O_{7-x}$ (YBCO)-edge surface was not exposed to solvent through all fabrication procedures. The barriers were produced by structural modification at the edge of the YBCO base electrode using high energy ion-beam treatment prior to deposition of the YBCO counter electrode. We investigated the effects of high energy ion-beam treatment, annealing, and counter electrode deposition temperature on the characteristics of the interface-controlled Josephson junctions. The junction parameters such as T_c, I_c, R_N were measured and discussed in relation to the barrier layer depending on the process parameters.

Keywords : Josephson junctuions, ramp-edge junction, ion-beam treatment, $YBa_2Cu_3O_{7-x}$, Sr_2AlTaO_6, multilayer.

I. Introduction

High temperature superconducting (HTS) Josephson junctions are the important elements of superconducting device applications, such as superconducting quantum interference device (SQUID) magnetometers, voltage standards, and single flux quantum (SFQ) logic circuits. These applications require junctions that have critical currents (I_c) in the range 100~500 μA, normal resistance (R_N) values of one to several ohms, and inductances of several pH, with 1-σ spread less than 10%. Ramp-edge Josephson junctions are promising candidates for HTS SFQ digital circuits rather than the other junctions[1,2]. Recently, there was a breakthrough improving the reproducibility and uniformity of the junctions by the interface-engineered junction technique[3]. In this junction, the barrier was formed on a ramp-edge surface of $YBa_2Cu_3O_{7-x}$ (YBCO) base electrode by structural modification using vacuum annealing and *in-situ* plasma treatment at high substrate temperature prior to the deposition of the counter electrode. Instead of plasma treatment, the barriers were fabricated by using an ion-beam damage at elevated temperatures or using a chemical treatment[4~6]. However, the uniformity is still not sufficient for applications of SFQ digital circuits.

Although $SrTiO_3$ is known as a conventional insulating materials for the HTS multilayer process, it has a too large dielectric constant for high frequency applications. In contrast, the dielectric constant reported for SAT films of ε = 23~30 indicates that it is an excellent choice for high-speed digital circuits[7]. In our process, Sr_2AlTaO_6 (SAT) layer was used as an ion-milling mask as well as an insulating layer for the ramp-edge junctions. In 2-step ion milling process using SAT as an etching

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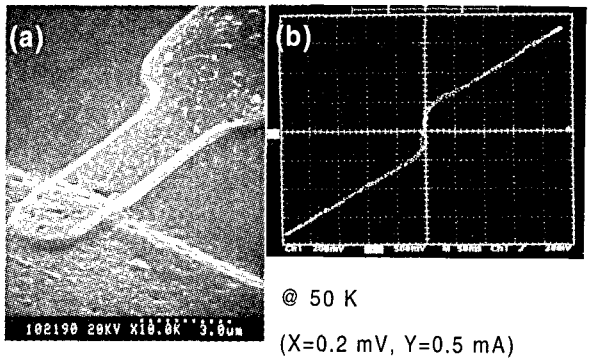
mask, an ion-milled YBCO ramp-edge was not exposed to solvent through all fabrication procedures.

In this study, we have investigated the optimization of the deposition conditions for the YBCO base electrode layer and Sr_2AlTaO_6 (SAT) layer which was used as an ion-milling mask as well as an insulator. The effects of the vaccum annealing after ion-beam damage and the YBCO counter electrode deposition temperature on the junction parameters were also investigated.



@ 50 K

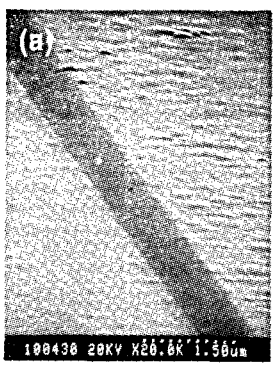
(X=0.2 mV, Y=0.5 mA)

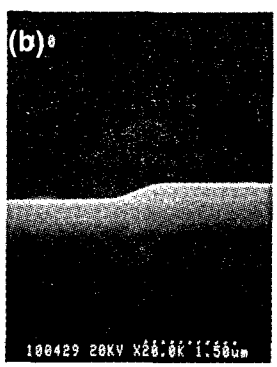
II. Experimental procedure

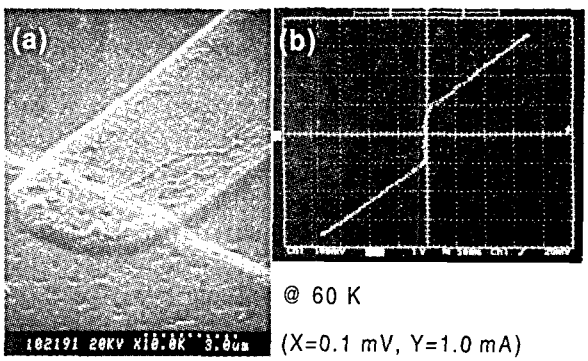
Our process for fabricating junctions was based on a 2-step ion milling process, in which the etching mask was not a PR but a patterned SAT layer on the YBCO base electrode. YBCO, SAT, and Au for contact pads were deposited by KrF PLD on $LaAlO_3$ (LAO) (100) single crystal[8]. The energy density of the laser beam on the target, the oxygen pressure in the chamber, the substrate temperature, and the substrate to target distance were varied to optimize the thickness, the surface roughness, and the film quality[9]. The YBCO layer was deposited in 100 mTorr oxygen at about 820 ℃. The SAT layer was grown at the substrate temperature of 700 ~ 780 ℃ and the oxygen partial pressure of 100 mTorr. The target-substrate distance for YBCO layer deposition was 6.5 cm. The distance for the growth of SAT was 5.5 ~ 6.5 cm. YBCO electrode and SAT insulating layer were deposited sequentially on the substrate.

The SAT layer was patterned using 350 V and 30 mA Ar ion-milling with a reflowed AZ5214 PR mask. The substrate was rotated during the ion-milling. After the PR was removed, the ramp-edge was etched by second-ion-milling using the SAT mask. The final angle of the ramp-edge was about 21° from the substrate surface as shown in Fig.1.

After making the ramp-edge, the ramp-edge was damaged by high voltage ion-beam of 700 V. Following the ion-beam damage, the samples were annealed at 500, 600, 700 °C under an oxygen pressure of 400 mTorr for 30 min. before depositing the YBCO counter electrode and SAT insulator by PLD. The counter electrode was patterned by ion-







@ 60 K

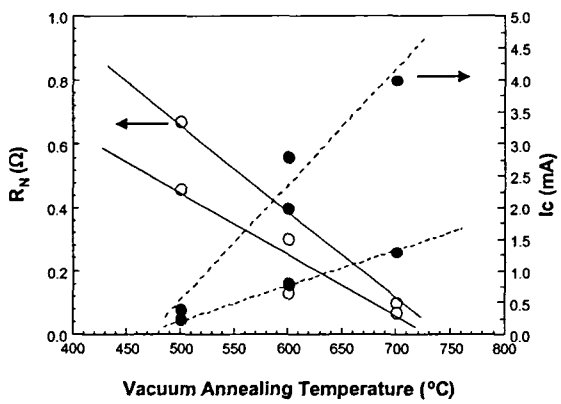
(X=0.1 mV, Y=1.0 mA)

milling to define the junction width. Finally, Au was also deposited by PLD and patterned by lift-off for the contact pads.

III. Results and discussion

We fabricated the 5x5 mm^2 test chip including the micro-bridge patterns of YBCO base and counter electrodes, two pairs of 2 μm and 5 μm-wide junctions having a common base electrode. Fig. 2 (a) shows a scanning electron micrograph of the well-defined 2μm-wide junction annealed at 500 °C under an oxygen pressure of 400 mTorr for 30 min before depositing the YBCO counter electrode. Its I-V characteristic showed RSJ-like behavior and an I_c of 0.4 mA and R_N of 0.67 Ω at 50 K, yielding an I_c R_N product of 0.27 mV as shown in Fig. 2(b). On the other hand, a 5μm-wide junction annealed at 600 °C under the same condition as the 2μm-wide junction had an I_c of 1.0 mA and R_N of 0.15 Ω at 60 K, yielding an I_c R_N product of 0.15 mV as shown in Fig. 3(b).

The crystalline state of the barrier layers formed by the ion-beam damage depends on the vacuum annealing temperature. As shown in Fig. 4, the R_N value decreased and the I_c value increased with increasing vacuum annealing temperature prior to counter electrode deposition. We learned that the ion-beam damaged layer could be transformed to a stable and resistive barrier layer by vacuum annealing at 500 °C. The largest R_N was 0.67 Ω, which is not sufficient for digital circuit applications. It was due to the fact that the ramp-edge surface damaged by high voltage ion-beam not at an elevated temperature but at room temperature. In addition, the barrier layer depends on counter electrode deposition temperature. At the same vacuum annealing temperature, the junctions fabricated at the lower counter electrode deposition temperature showed higher R_N. The I-V characteristics showed RSJ-like behavior and the critical temperature of the junctions were above 83 K. The 2 μm-wide junction had an I_c of 0.4 mA and R_N of 0.67 Ω at 50 K.



IV. Summary

The deposition conditions of the YBCO base electrode and SAT insulating layer have been optimized. In the 2-step ion milling process, an ion-milled YBCO ramp-edge was not exposed to solvent through the fabrication process. The ion-beam voltage, ion-beam incident angle, PR mask angle, and PR reflowing temperature were optimized to obtain the ramp-edge with a smooth surface and an angle of about 21°. We learned that the ion-beam damaged layer could be transformed to a stable and resistive barrier layer by vacuum annealing at 500 °C. In addition, the barrier layer depended on the counter electrode deposition temperature. The I-V characteristics of the interface-controlled junctions fabricated in this work showed RSJ-like behavior and the critical temperature of the junctions were above 83 K. The 2 μm-wide junction had an I_c of 0.4 mA and R_N of 0.67 Ω at 50 K, yielding an I_c R_N product of 0.27 mV.

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