Improvement in Electrical Stability of poly-Si TFT Employing Vertical a-Si Offsets

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Abstract

Polycrystalline silicon (poly-Si) thin film transistors (TFT's) employing vertical amorphous silicon (a-Si) offsets have been fabricated without additional photolithography processes. The a-Si offset has been formed utilizing the poly-Si grain growth blocking effect by thin native oxide film during the excimer laser recrystallization of a-Si. The ON current degradation of the new device after 4 hour's electrical stress was reduced by 5 times compared with conventional poly-Si TFT's.

Introduction

Poly-Si TFT's are considered the most promising devices for AMLCD application.[1] However, poly-Si TFT's exhibit abnormally large OFF-state leakage current and have reported to degrade considerably due to the generation of additional trap states in the poly-Si channel, which are caused by the presence of high carrier densities in the ON-state.[2), 3)] We present a new device structure to reduce the large leakage current and to improve the electrical stability of poly-Si TFT's. The device has vertical a-Si offsets that are formed during the excimer laser recrystallization of the channel poly-Si without additional photolithography processes. In the OFF-state, the highly resistive a-Si offsets reduce the electric field in the drain depletion region. In the ON-state, current flows through broad cross-sections of the a-Si offsets and the current density in the depletion region near the drain is significantly reduced. Therefore the generation of additional trap states is reduced and the stability of the device is improved.

Experiments

Fig. 1 shows the device structure of the proposed poly-Si TFT. In the ON-state, the current flow passing through the vertical a-Si offsets and poly-Si channel as indicated by the dotted arrow line. The current in the longitudinal edge of the channel flows spreading downward as shown in Fig. 2. The cross-sectional area of the a-Si offset through which current flows is much broader than the poly-Si channel cross-sectional area, and the current density in the a-Si offset decreases.

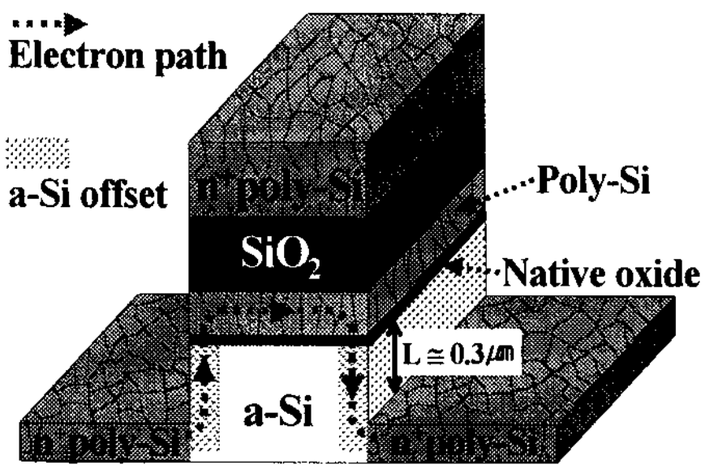
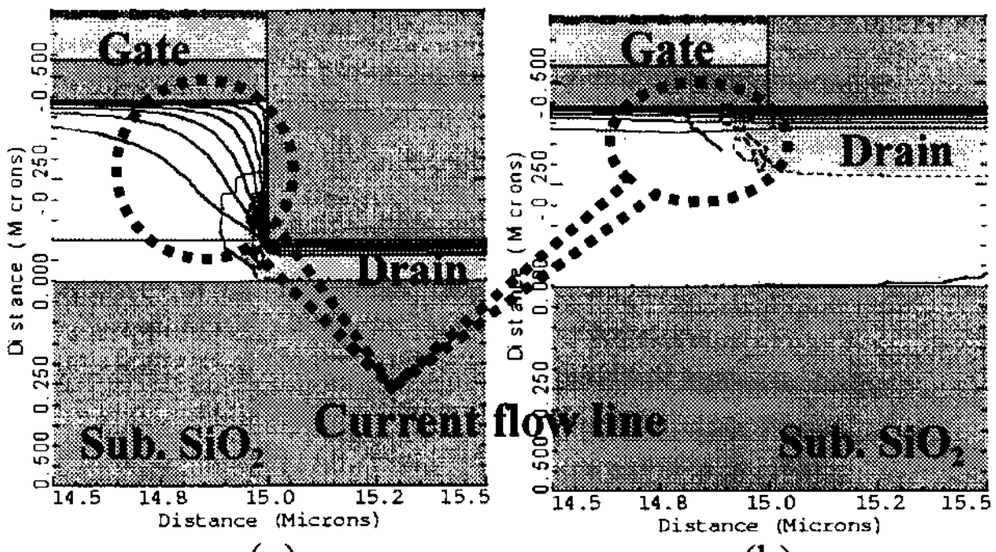


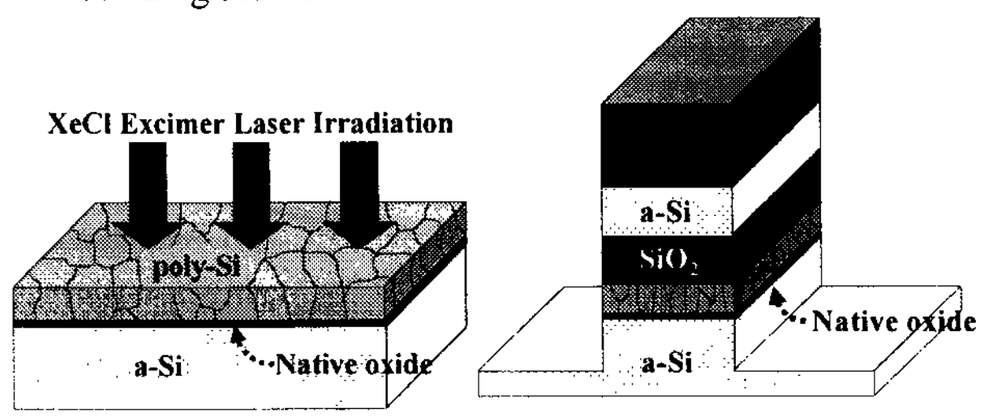
Fig. 1 Poly-Si TFT with vertical a-Si offset. L_{offset}=0.3㎛.

Key process steps are shown in fig. 3 and as follows. Fig 3. shows the key process steps of the new TFT. Undoped a-Si film was deposited on oxidized Si-wafer. A thin native oxide film was formed on the upper surface of the a-Si during the cleaning process. Then, an a-Si film was deposited again. XeCl excimer laser (λ=308㎚) was irradiated and the upper a-Si film was recrystallized (Fig. 3 (a)). The formation of a poly-Si/a-Si double film structure was observed by TEM as shown in Fig. 4-(a). A TEOS gate insulator and a-Si film for gate electrode were deposited and patterned. Before removing the PR, the poly-Si film and the a-Si film for source/drain region were also etched for the formation of the vertical a-Si offsets (Fig. 3 (b)).



(a) (b)

Fig. 2. Current flow line in the new TFT (a), and in the conventional top-gate TFT (b). Simulation was carried out utilizing the MEDICI.



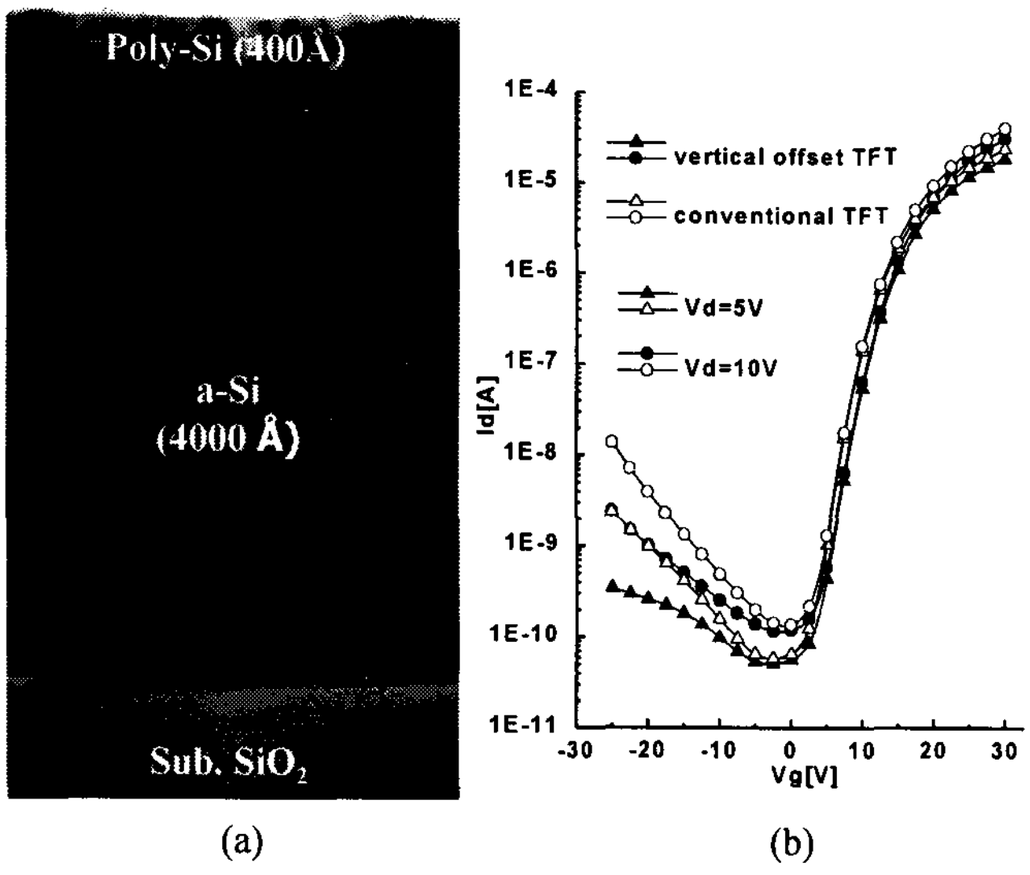
(a) (b)

Fig 3. Key process steps of the new poly-Si TFT. Recrystallization of upper a-Si film by XeCl laser (a). Vertical a-Si offset formation after patterned (b).

Results and Discussions

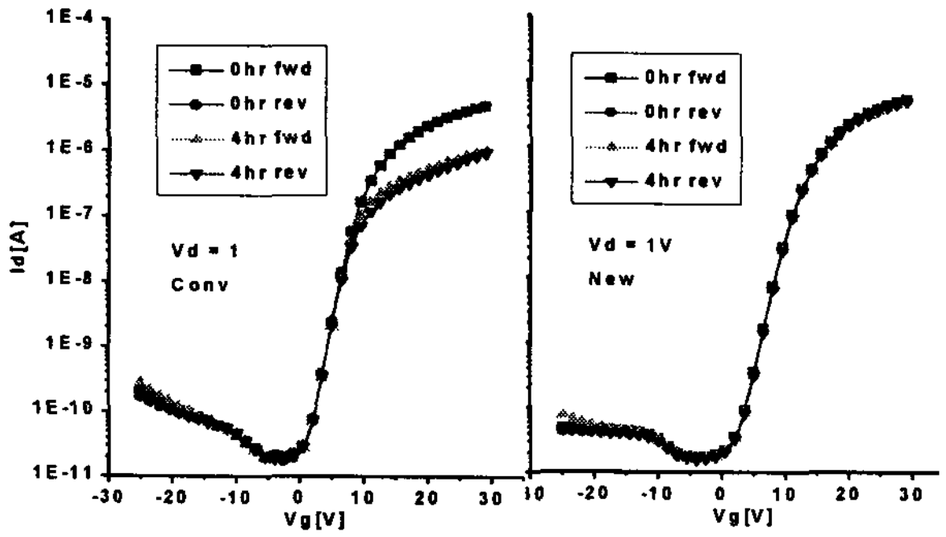
Fig. 4-(a) is the cross-sectional TEM image of the poly-Si/a-Si double film structure fabricated by the excimer laser irradiation on the a-Si/native silicon oxide/a-Si film. Due to the crystallographic differences between silicon and silicon oxide, the successive grain growth of poly-Si is blocked at the thin oxide and the lower a-Si can be preserved if it has sufficient thermal capacity. Fig. 4-(b) shows the measured transfer characteristics of the poly-Si TFT's with and without vertical a-Si offsets. W_{CH}/L_{CH}=10㎛/10㎛

and L_{offset}= 0.3μm. It is observed that the poly-Si TFT's with vertical a-Si offsets exhibit smaller leakage current compared with the conventional poly-Si TFT due to the decrease of the drain field by the a-Si offsets.[4)]

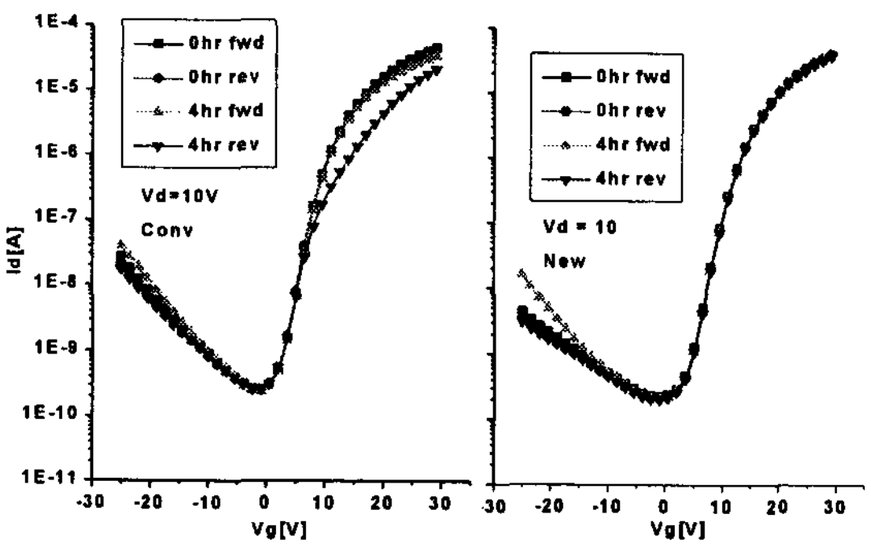


(a) (b)

Fig. 4 (a) Cross-sectional TEM image of the poly-Si/a-Si double film structure. The laser energy density is 230mJ/㎠. (b) Transfer characteristics of poly-Si TFT with vertical a-Si offsets. W/L=10μm/10μm.



(a)



(b)

Fig. 5. Transfer characteristics of the vertical a-Si offset TFT and the conventional TFT before and after electrical stress of V_{DS}=V_{GS}=30V for 4 hours. V_{DS}=1V (a). V_{DS}=10V (b).

Due to the highly resistive a-Si offset, the threshold voltage ($V_{TH\cdot NEW}$=12.4V) and the subthreshold slope (S_{NEW}=2.06V/dec) of the new device are slightly larger than those ($V_{TH\cdot CONV}$=11.7V, S_{CONV}=1.97V/dec) of conventional devices. However, the maximum ON/OFF current ratio that is the most important characteristic as a pixel-switching device is improved by more than five times. Poly-Si TFT's degrade primarily due to the generation of additional trap-states which are caused by large current drive for a long period. The degradation occurs more rapidly when the device is in saturation and there is a high channel electric field near the drain.[2)] Therefore the defect creation occurs mainly in the drain depletion region of the poly-Si channel and the stressed device exhibits asymmetric electrical characteristics due to the potential barrier built from the charged traps. Fig. 5 shows the transfer characteristics of the vertical a-Si offset TFT and the conventional TFT before and after electrical stress of V_{DS}= V_{GS}=30V for 4 hours. The new poly-Si TFT exhibits excellent stability with respect to the ON current sustaining capability after the stress. The ON current degradation after the stress has been improved by 20 ~ 80 % compared with the conventional TFT as listed in table 1. This result is due to the decrease in the current density in the drain depletion region of the new TFT. For a small V_{DS}, the conventional device exhibits symmetrical transfer characteristics (Fig. 5 (a); V_{DS}=1V). However for larger V_{DS}, serious asymmetry appears between the reverse and forward mode characteristics due to additionally created potential barrier in drain side (Fig. 5 (b); V_{DS}=10V).

Table 1. The ON current maintenance after electrical stress

(I_{ON} after stress/ I_{ON} before stress)

V_{DS}	Conventional TFT		a-Si offset TFT	
	Rev.	Fwd.	Rev.	Fwd.
10V	40%	78%	91.0%	96.0%
5V	36%	57%	92.5%	93.5%
3V	30%	41%	93.0%	94.0%
1V	19%	21%	93.4%	93.5%

Conclusions

We have fabricated poly-Si TFT's with vertical a-Si offsets between the channel and the source/drain. Due to the a-Si offsets, the OFF-state leakage current is reduced and the maximum ON/OFF current ratio of the new TFT increased by more than 5 times compared with the conventional poly-Si TFT. The stability of the new TFT was improved by 5 times employing the vertical a-Si offset, because the current density in the drain depletion region is reduced and the additional trap generation is prevented. The excellent stability of the new TFT may guarantee long-term reliability for high-resolution AMLCD applications.

References

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