Optimized Gate Driving to Compensate Feed-through Voltage for C_{ST}-on-Common

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Abstract

In recent years, attempts have been made to greatly improve the display quality of active-matrix liquid crystal display devices, and many techniques have been proposed to solve such problems as gate signal delay, feed-through voltage and image sticking[1-3]. To improve these problems which are caused by the feed-through voltage, we have evaluated new driving methods to reduce the feed-through voltage. Two level gate-pulse was used for the gate driving of the cst-on-common structure pixels. These gate driving methods offer better feed-through characteristics than conventional simple gate pulse. Optimized step signal will compensate by step pulse time and voltage. The evaluation of the suggested driving methods were performed by using a TFT-LCD array simulator PDAST which can simulate the gate, data and pixel voltages of a certain pixel at any time and at any location on a TFT array. The effect of the new driving method was effectively analyzed.

Introduction

Hydrogenated amorphous silicon thin film transistors are used as a pixel switching device of TFT-LCDs and very active works on a-Si:TFTs are in progress. Further development of the technology based on a-Si:H TFTs depends on the increased understanding of the device phsics and the ability to accurately simulate the characteristics of them. A user-interactive pixel design tool for high-quality TFT-LCDs is realized and used to explore the sensitivity of the various array and device parameters for optimizing pixel design. In this tool, the electrical characteristics such as gate, data, pixel and feed-through voltage can be analyzed. This analysis of driving method will be utilized effectively.

Pixel Charging Characteristics

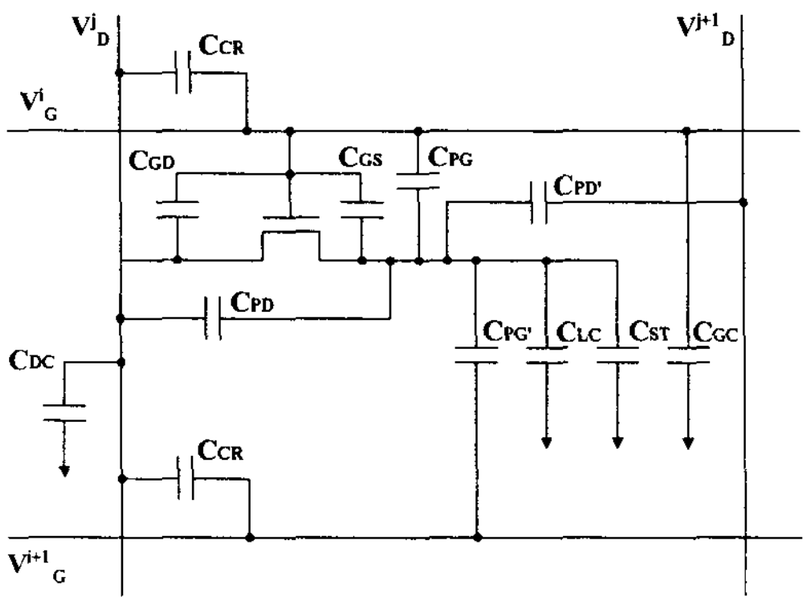

Figure 1 . Equivalent Circuit of CST-on Common

Pixel of TFT-LCD will show equivalent cirsuit by Liquage Capacitance(C_{LC}), Storage Capacitance(C_{ST}), and Gate-to-Source Overlap Capacitance(C_{GS}) in figure 1.

This circuit will simulate by consider gate line to pixel electrode capacitance(C_{PG}), adjacent gate line to pixel electrode capacitance(C_{PG}`), data line to pixel electrode capacitance($C_{PD}$), adjacent data line to pixel electrode capacitance($C_{PD}$`). $v_P(t)$ is pixel electrode voltage, $v_G(t)$is gate voltage and $v_D(t)$ is data voltage. Linear region , saturation region and off region of TFT output characteristics is

Linear region : $v_G(t) > v_D(t) + V_{th}$

$$i_D = \beta_0 \cdot \{[v_G(t) - V_{th} - v_P(t)] \cdot [v_D(t) - v_P(t)] - \frac{[v_D(t) - v_P(t)]^2}{2}\}$$

Saturation region : $v_G(t) \le v_D(t) + V_{th}$

$$i_D = \frac{\beta_0}{2} \cdot [v_G(t) - V_{th} - v_P(t)]^2$$

Off region : $v_G(t) < V_{th}$

$$i_D = I_{off}(v_D)$$

Gate Driving Method for Compensation of Feed-through Voltage

Reason of feed-through voltage is decreased of pixel voltage by charged carrier capacity variation in parasitic capacitance between gate electrode and data electrode by gate voltage variation. When RC delay is happened, feed-through voltage is decreased. This effect is caused for compensate, through drain electrode, decrease of parasitic condenser carrier capacity in TFT channel active state, because gate voltage variation speed is decrease. Gate voltage is generally used simple pulse like figure 2(a). If two-step pulse is used like figure.1(b) in used optimized step size and maintain time, we have voltage compensation effect in second voltage drop unlike gate voltage drop at once.

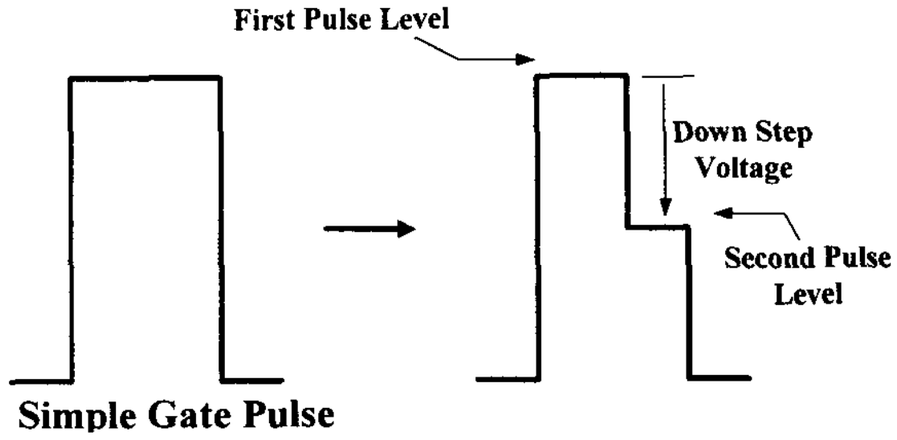

Figure 2. Gate Driving Method for Compensation of Feed-through Voltage

Simulation Result

When gate is drived on applied two-step voltage , the effect of feed-through voltage compensation is happened. We find pixel voltage and its compensate effect by size of second voltage drop on two-step voltage applied.

Simulation of pixel voltage by applied down-step voltage size is show in figure 3. Data voltage is 10V. Gate voltage is 20V at Start and 2V, 4V, 6V down-step voltage is applied at 20V after 30us. At first, feed-through is appear by gate voltage down-step and first feed-through voltage is decrease by down-step voltage increasing. If gate voltage is drop from second pulse level to off state after down-step of first gate voltage, pixel voltage is no more drop like simple gate pulse applied. Consequently, pixel voltage is compensated about 16% to not matter second pulse voltage.

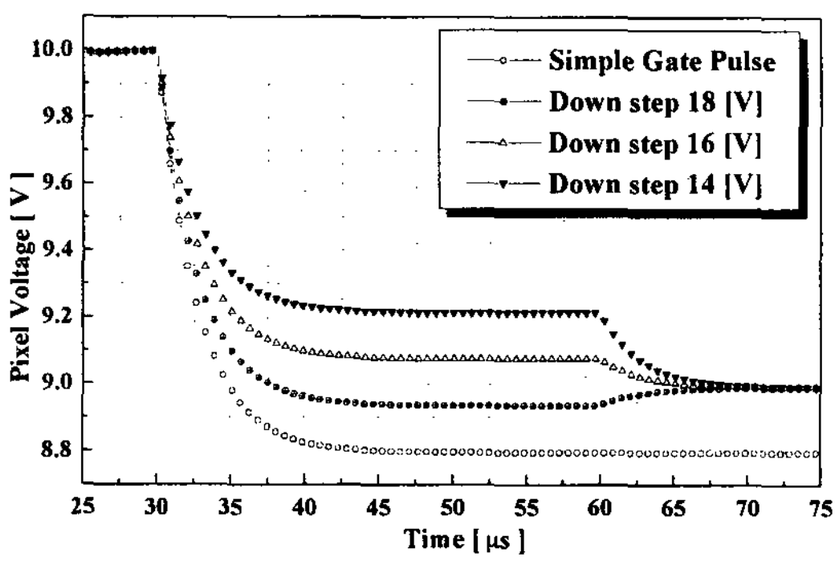

Figure 3. Feed-Through of Pixel Voltage
by Change Down Step Voltage

We have simulated gate voltage width (figure 4.). Gate voltage width simulated from 5μs to 15μs. We know that gate voltage width will have minimum 13μs for 98% charging ratio. And we simulated feed-through voltage for gate voltage width (figure 5.) The shorter charging time, the feed-through voltage is decreased . Then we will consider to feed-through voltage to 13μs gate voltage width for 98% charging ratio.

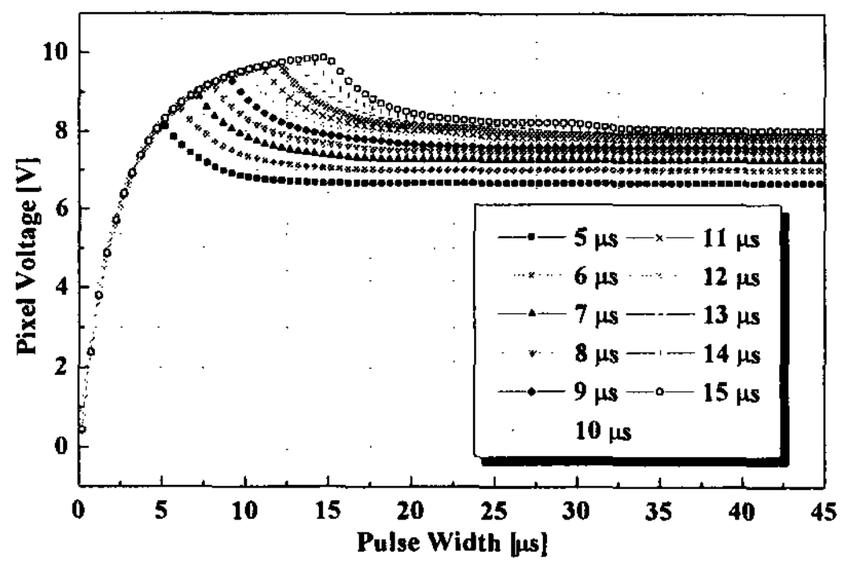

Figure 4. Pixel Voltage of Gate Voltage Width

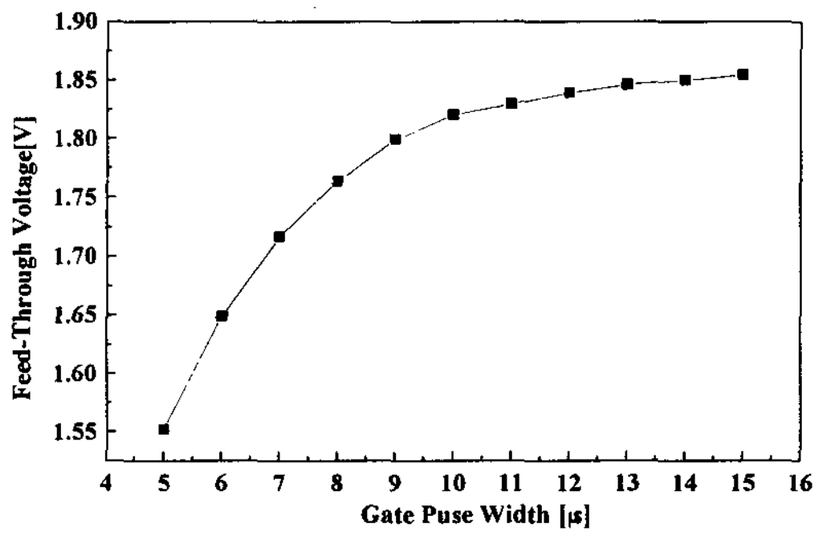

Figure 5. Feed-Through Voltage of Gate Voltage Width

Conclusion

we have evaluated new driving methods to reduce the feed-through voltage. Two level gate-pulse was used for the gate driving of the cst-on-common structure pixels. These gate driving methods offer better feed-through characteristics than conventional simple gate pulse. Optimized step signal voltage and width compensated to step pulse time. The evaluation of the suggested driving methods were performed by using a TFT-LCD array simulator PDAST which can simulate the gate, data and pixel voltages of a certain pixel at any time and at any location on a TFT array. At next user will evaluate at any gate driving method.

Acknowledgement

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Reference

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