Addressing conditions to transfer optimum surface discharge in ac PDP

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Abstract

This paper deals with the relationship between the addressing and the display in ac-PDP. Especially, deals with the transfer probability of surface discharge according to addressing voltage (Va), blocking voltage(Vg) in addressing period and the characteristics of luminance according to sustain voltage(Vs) in sustaining period with ADS(Address Display period Separation) driving method.

Introduction

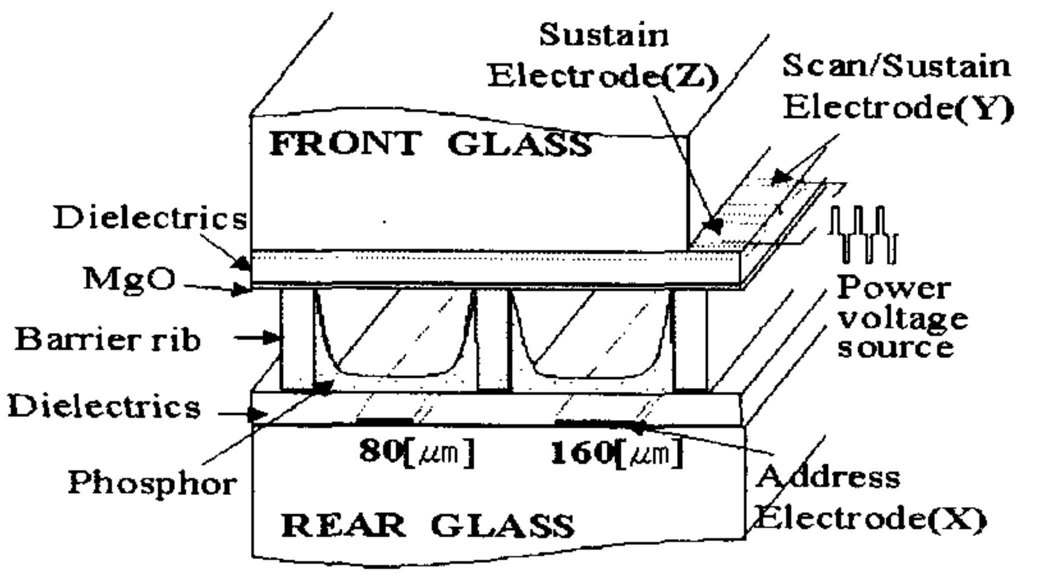


Fig. 1 The schematic diagram of ac-PDP

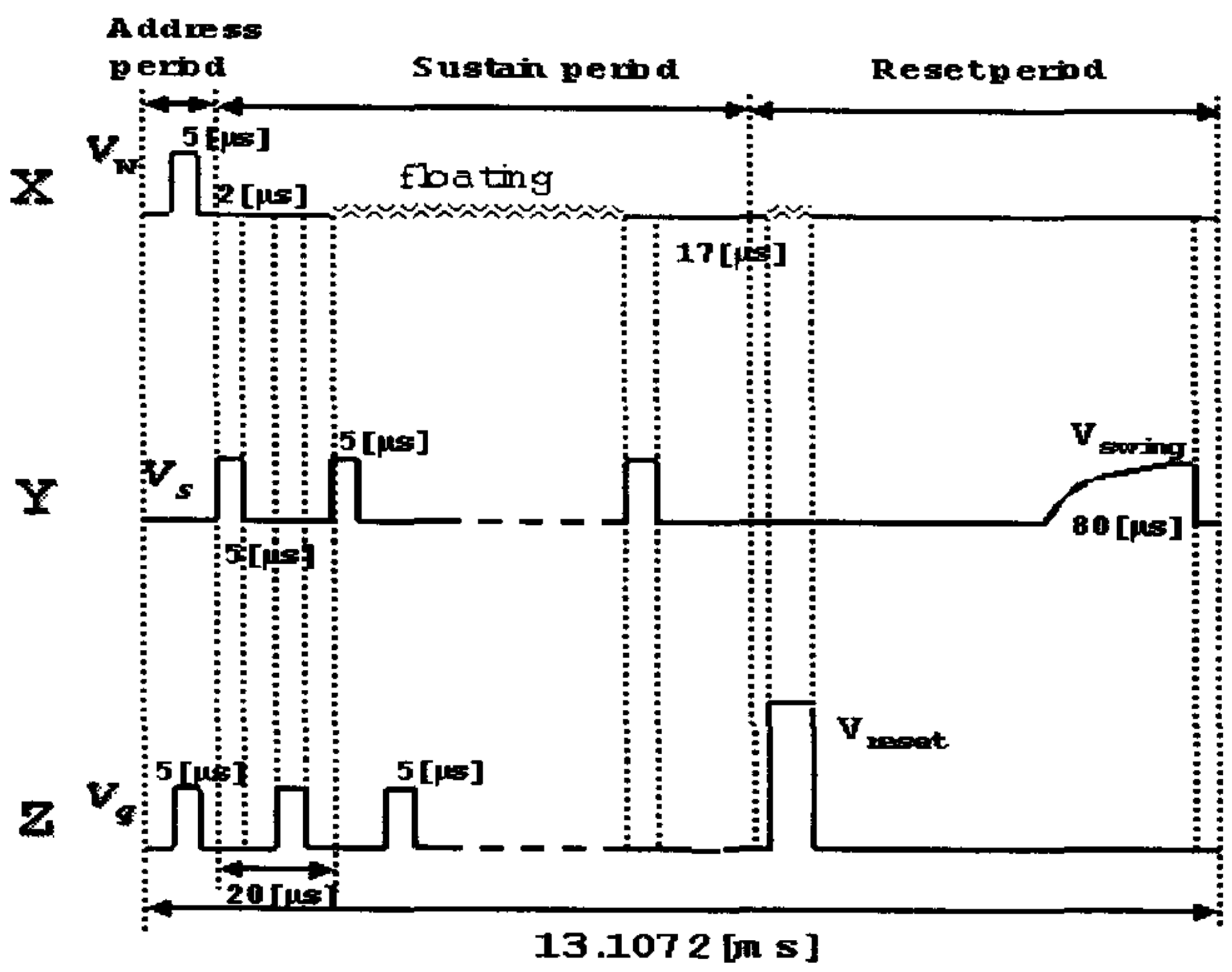


Fig. 2 Experimental time chart

Figure 1 shows the schematic diagram of ac-PDP.[1]

Figure 2 shows the driving voltage waveform used in this experiment. This consists of 3 periods. In reset period, all cells are in a same condition. In the address period, address discharge voltage is determined by address voltage (Va) and blocking voltage (Vg). After the address discharge, surface discharge is initiated.

In this study, the address conditions to transfer optimum surface discharge in ac PDP have investigated as a parameter of addressing discharge inception voltage (Va) between X and Y electrodes that lead to the surface discharge, blocking voltage (Vg) of Z electrode in order to block the discharge between X and Z electrode, and sustain voltage(Vs) between Y and Z electrodes.

Experiment

Figure 3 shows the schematic diagram of discharge chamber to test the characteristics of discharge. He-Ne(30%)-Xe(2%) mixture gas is filled to 300[Torr]. The sustain voltage (Vs) is selected as a value between firing voltage and sustain voltage of surface discharge. And then, the reset voltage (Vreset) and the swing voltage(Vswing) are fixed.

The minimum address voltage (Va) is under a given blocking voltage(Vg) is measured by progressively increasing applied voltage until sustain discharge at the selected cells with 50[kHz] square wave voltage. As a parameter of Va,, Vg and Vs in three electrode, we investigated the addressing probability and relationship among Va, Vg and Vs

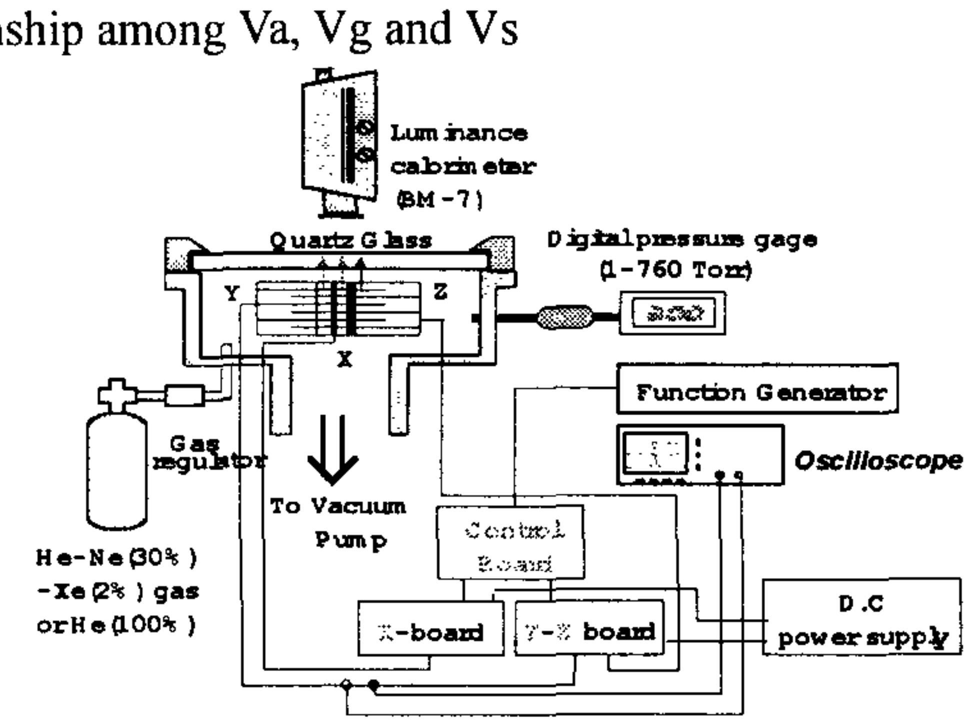
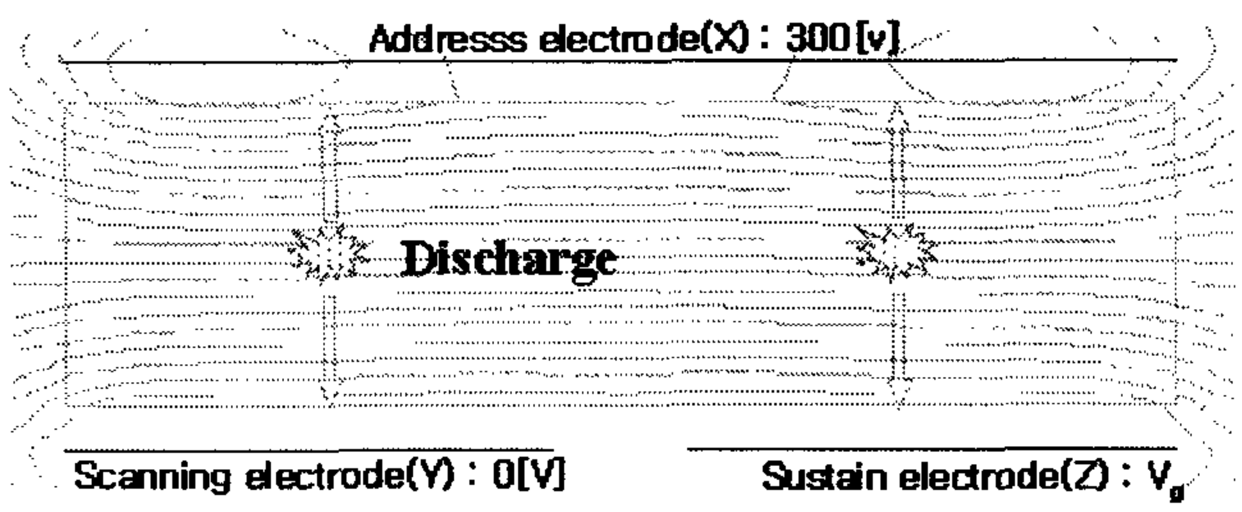
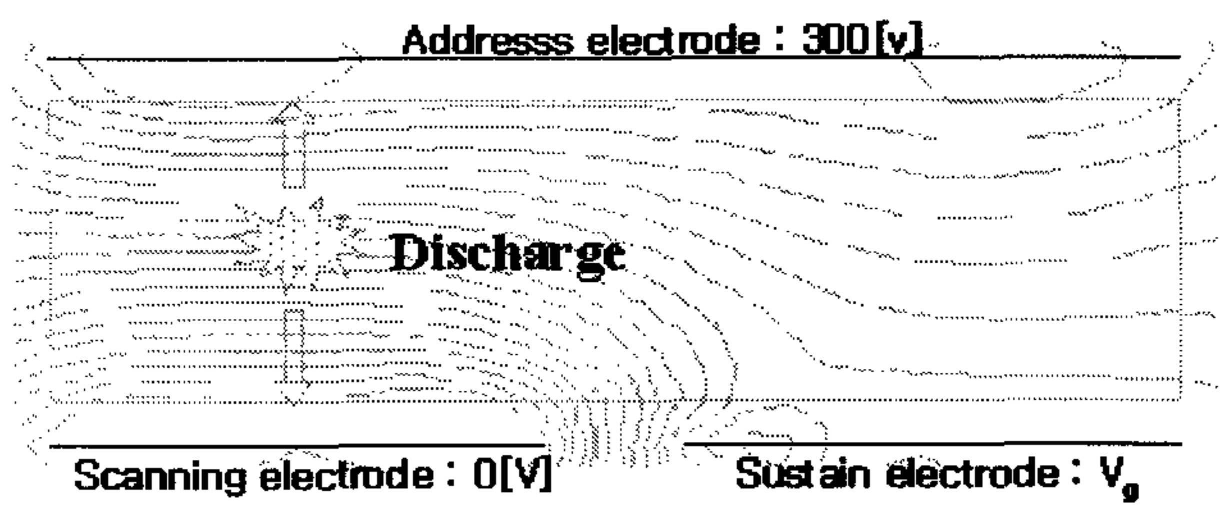


Fig. 3 The schematic diagram of discharge test chamber

Results and Discussion



(a) The characteristics of equi-potential when Vg is 0[V].



(b) The characteristics of equi-potential when Vg is **200** [V]

Fig. 5 The characteristics of equi-potential diagram

Figure 5 shows the characteristics of equi-potential diagram as a parameter of Vg in address period. Figure 5(a) is obtained under the conditions of Va=300V and Vscan=Vg=0. Fig 5(a) is obtained at Va=300V, Vg=200V and Vscan=0V. Since the electric field at the edge of scanning electrode increases with the blocking voltage Vg , the charged particles accumulates on the edge. As a result, the address probability to transfer surface discharge may be increased.

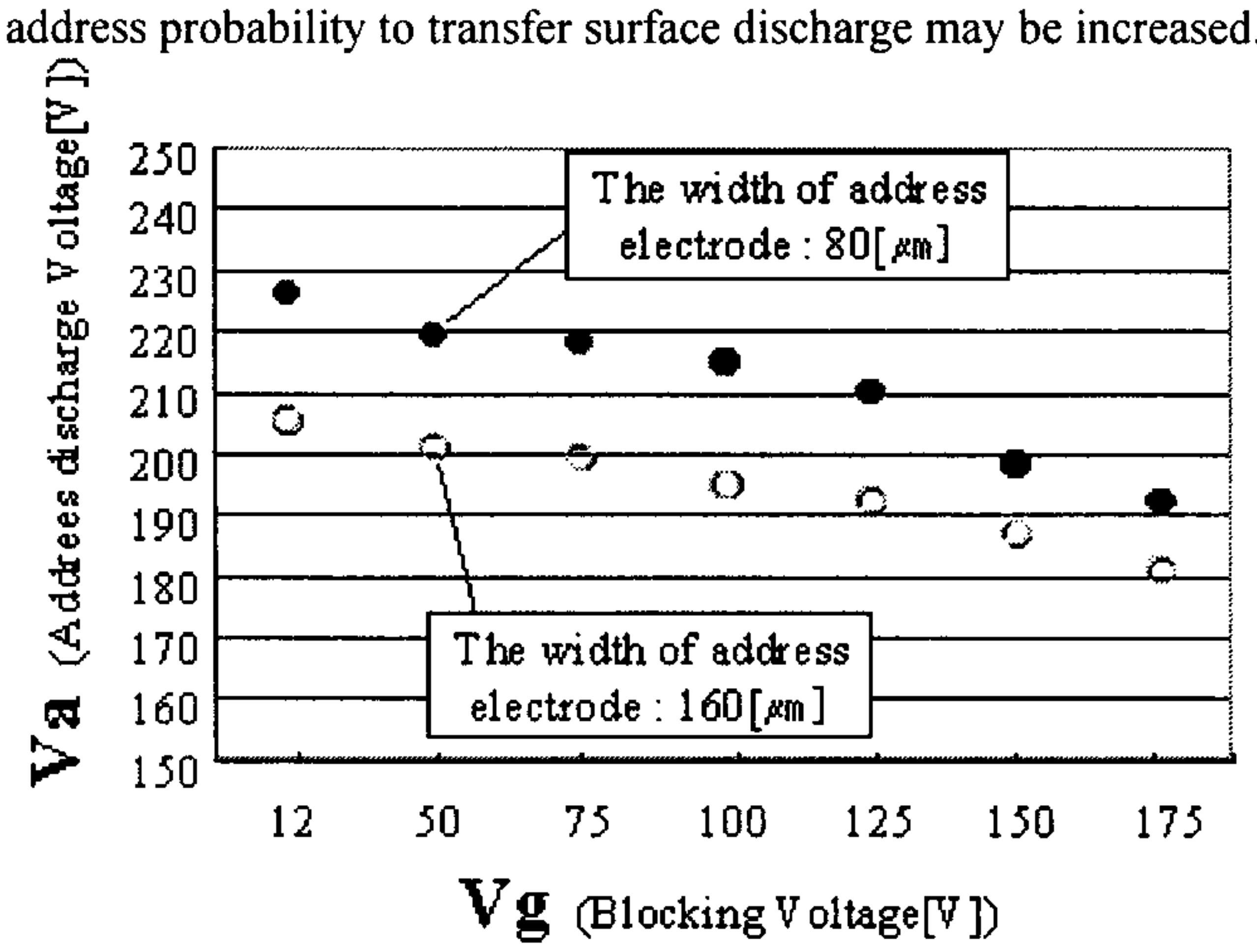


Fig. 6 The characteristics of relationship between Va and Vg

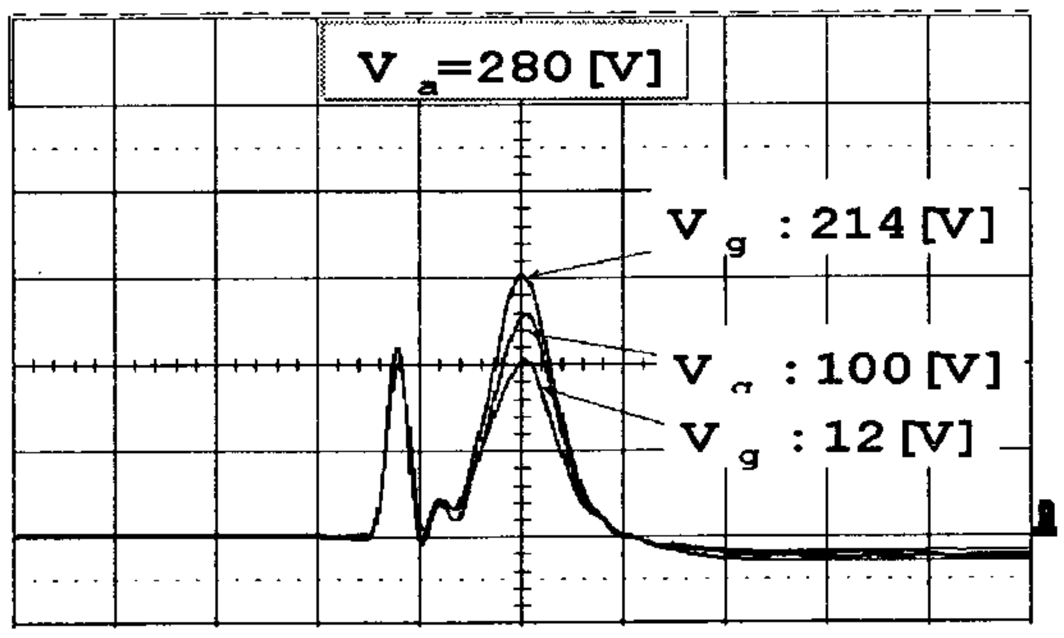
Fig 6 shows the relationships between Va and Vg as a parameter of the width of address electrodes. The measured points in the figure shows the addressing discharge inception voltage at a given Vg to transfer surface discharge with a 100 % probability under the conditions of Vs=180[V], Vswing=160[V] and Vreset=350[V]. From this figure it can be noticed that Va is decreased with increase in Vg, regardless of the address electrode width. The reason may be explained as follows.

The polarity of blocking voltage of Z electrode is the same with X electrode. Furthermore, the opposite polarity charges are induced at the edge of Y electrode that is located near "Z" electrode. Therefore, these opposite polarity charges lead to low addressing and sustain discharge inception voltage. However, the wider the address electrode width, the lower the addressing inception voltage (Va) at a given Vg.

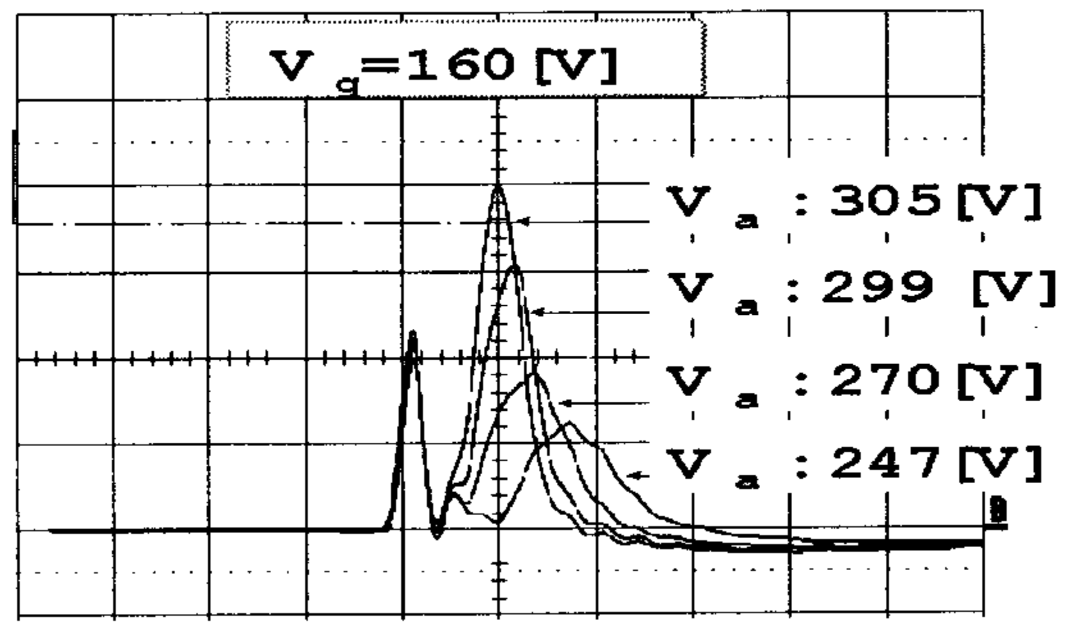
If Vg is greater than the firing voltage of the surface discharge, unselected cells are discharged. Therefore Vg is controlled from 0 to 195[V] to prevent misfiring. And if the applied voltage becomes higher than 350[V], misfiring happen. There is an upper limit of Va if Va is too large. Therefore, it is possible that self-erasing (SE) partly erase the charges deposited during addressing of the cell, or other cells sharing the same address electrode are affected by the address pulse applied to turn on a particular cell. Their lower or upper limits of the address voltage define the margin of the address voltage.[3]

Figure 7(a) shows the characteristics of current waveform as a parameter of overvoltage Vg and Va in address electrode. Figure 7(a) shows that first and second current peak is displacement current. Third current peak is the discharge current. The part of discharge current is increased with the Vg under the constant Va and Vs. The discharge current is also increased with Va under the constant Vg and Vs

Fig 8 shows the characteristics of luminance as a parameter of Vs. The range from 160 to 190[V] is the sustain voltage range which is possible to use memory function.



(a) Current waveform as Va increases



(b) Current waveform as Vg increases

Fig.7 Current waveform as a parameter of Vg and Va

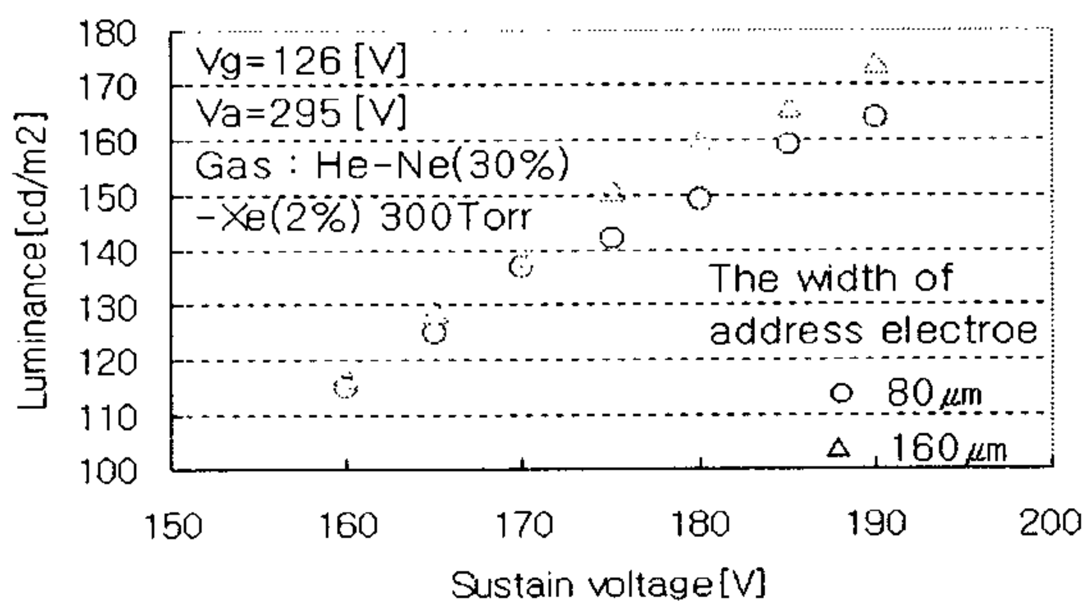


Fig. 8 The luminance as a parameter of Vs

The characteristics of luminance are measured in condition that all the selected cells are turned on. As sustaining voltage increases, luminance is also increased. Furthermore, luminance is also increased as the width of address electrode increase.

Conclusions

The addressing discharge inception voltage (Va) that transfer surface discharge with a 100 % probability is decreased with increase in the blocking voltage Vg regardless of the address electrode width. The reason is due to the induced charges at the edge of Y electrode by Vg. Furthermore, the wider the address electrode width, the lower the addressing inception voltage at a given Vg. Under the condition of the overvoltage on the address electrodes, the discharge current is increased significantly, whereas the discharge lag is decreased.

References

[1] C. Punset, *Journal of Applied Physics*, vol. 83

[2] Shahid Rauf, *Transaction on plasma science*, vol. 27. 1999

[3] C. Punset, *Journal of Applied Physics. 86*, No. 1, pp. 124-133