Discharge Characteristics of Addressing Period in the ADS driving scheme of AC-PDP

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Abstract

The understanding of reset scheme is essential for the driving of AC PDP (Plasma Display Panel). The characteristics of reset period of AC PDP was examined with the variation of pulse time and voltage in the ADS (Address Display Separated) driving method presented by Fujitsu,. The addressing characteristics showed drastic change as a function of the erasing time and addressing pulse width. In this paper, these results were explained by the change of wall charge variation, and it was estimated with the currents through each electrode.

Introduction

In the driving of AC-plasma display panel, the wall charge takes important role in the discharge characteristics. For example, the wall charge lowers the sustain voltage and enables writing display data to AC PDP. In the driving method of AC PDP, the ADS driving method is typically used. The ADS driving method is composed of three parts; reset, address and sustain period (Fig.1). And reset period is composed of total writing and erasing period, and distributes adequate wall charge for the subsequent addressing period. As a results, the addressing characteristics are highly dependent on the discharge caused by writing pulse and erase pulse. We examined the change of addressing voltage as a function of erase pulse width and addressing time using 21" VGA AC PDP with Ne-3%Xe 500 Torr.

Experiments & Results

1. Erase Pulse Decay time and Address Voltage Relationship

To analyze the relation between address voltage and erase pulse decay time, we need fixed state before erase pulse. In Fig.1 there is 1 writing discharge and 1 sustain discharge before erase discharge. Fig. 2 shows the change of addressing voltage as a function of erasing time. The erasing pulse used in this experiment exponentially decreases from sustain voltage to zero volt. The change of erase pulse width means the change of exponential decay time of scan electrode voltage. As the width of erasing pulse increased, the addressing voltage decreased drastically.

In case of short erase pulse width, the total charge amount, which flows through the scan electrode, is quite large. On the contrary, charge amount in the long erase pulse is much smaller. Fig. 3 shows the amount of the total charge flows during applying the erase pulse.

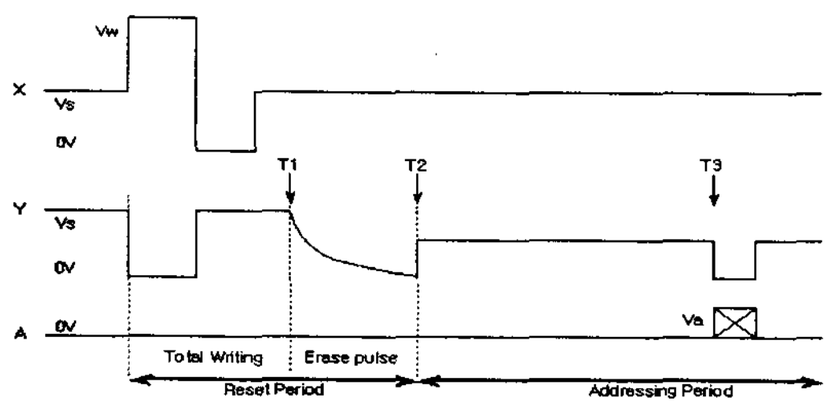

Fig. 1 ADS driving scheme

To analyze the result of the experiment of Fig.2 and Fig.3, there should be a few assumptions for the functions of each pulse. First, the address discharge in the scheme of Fig.1 is not a discharge which erases wall charge but which writes wall voltage. Second, because the sustain electrode and the address electrode are anodes and the scan electrode is cathode during addressing period, there should not be ordinary discharge in the erase discharge. If the erase discharge should take place in a large volume, the wall charge distribution will not be adequate for address discharge because built-up wall voltage will have reverse polarity. And, if the erase discharge should take place in too a small volume, the wall charge distribution will make a sustain discharge during sustain period in which the address discharge has not taken place.

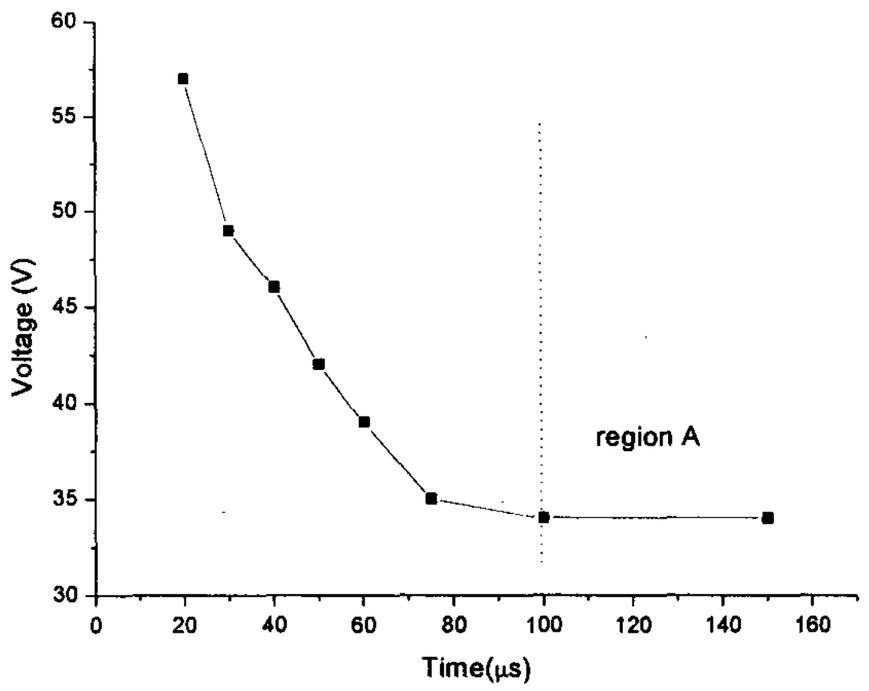

Fig. 2 The relation between the erase pulse width and the Address voltage

With these assumptions, the result of Fig.2 and Fig.3 makes itself explained. Slowly changing potential difference between the scan electrode and sustain electrode triggers discharge but not to the extend that brings about a discharge changing the polarity of the wall charge distribution. With short erase pulses, the voltage applied between the electrodes is apt to trigger the discharge of larger volume, and wall voltage is weakened more. So, only higher address voltage enables the address discharge. In long erase pulses, the voltage applied between the electrodes does not trigger much discharge, but the wall voltage is slightly lowered. So, even lower address voltage enables the address discharge. Still, the lowered wall voltage cannot make changing polarity discharge without help from the address voltage.

From Fig. 2, we also see that the address voltage does not change any more when the pulse width is sufficiently large (Region A). In the graph above, the value is 100us.

2. Scan Pulse width and address voltage relationship

Fig.4 shows the relation between the address voltage and the scan pulse width. $V_{add,\min}$ is the minimum voltage required to do

address voltage and $V_{add,\max}$ is the maximum voltage at which the writing error occurs in the discharge cell. The writing error occurs in the selected cells by self-erasing or in the unselected cell by a highly applied address voltage. From the graph, we see when the scan pulse width goes narrowly, the address voltage applied is to be set high.

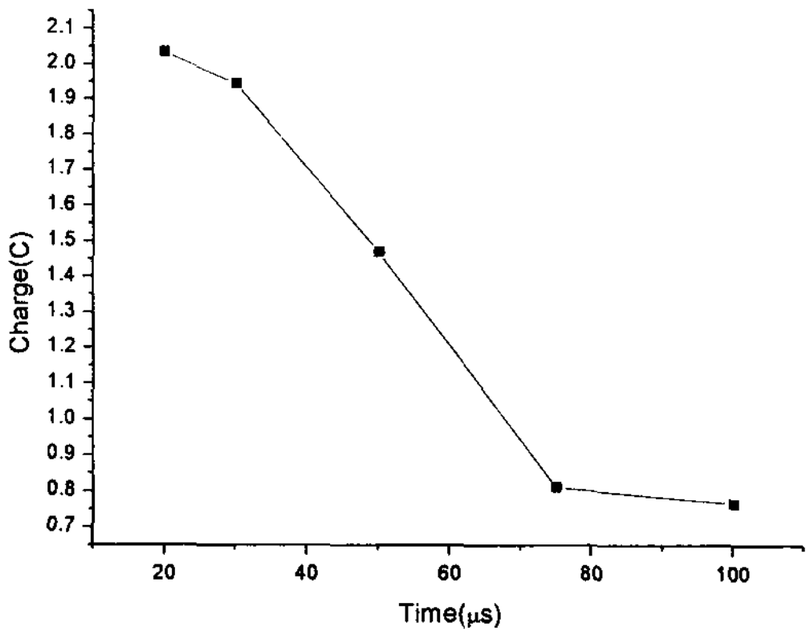

Fig. 3 Charge of the total charge during erase pulse is applied

Fig. 5 shows the current variation according to the change of the applied address voltage at the specific scan pulse width. The current peak has a delay about 0.5 ~ 1us with respect to the scan pulse applied to the scan electrode. As the address voltage goes to high, the amount of the current increases and the current peak delay decreases.

So, it can be said that it is required that the discharge current should flow sufficiently during applying the scan pulse for making write-discharge in the address period, and that for a sufficient current to flow through the electrode, higher address voltage is needed to decrease the discharge current delay.

On the contrary, when the address voltage is excessively high, the amounts of the current decreases because the self-erasing occurs. Fig. 6 shows the amounts of the charge flows during applying a scan pulse.

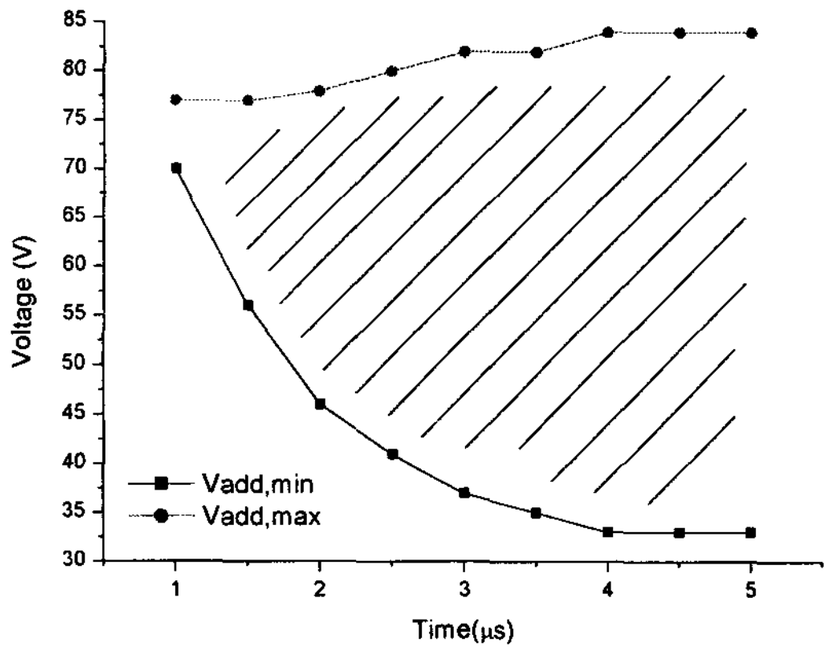

Fig. 4 Operation margin graph of address voltage

So, there exists an operational margin in the addressing voltage. That is, the voltage applied to the address electrode is to be a value between $V_{add,\min}$ and $V_{add,\max}$. When the scan pulse width is wide, the margin is large. But, when the scan pulse width is narrow, the margin is small.

Conclusion

In driving AC plasma display panel using ADS scheme, the correct use of wall charge and the wall voltage is important. So, it is very important to control the wall charge in the reset period by the total writing and erasing process. In the erasing period, we see that an erasing pulse having sufficient pulse width is to be applied to get high wall voltage to lower address voltage in the address period, and the erase pulse can be optimized in time because the wall voltage is fixed as constant in the small dv/dt region of the erase pulse. We can also see that the address discharge have "delayed" discharge characteristics, and there exists an operation margin in the address voltage. So, when driving AC-PDP, the operation point in the address period is set in the shadowed-region in the Fig. 4

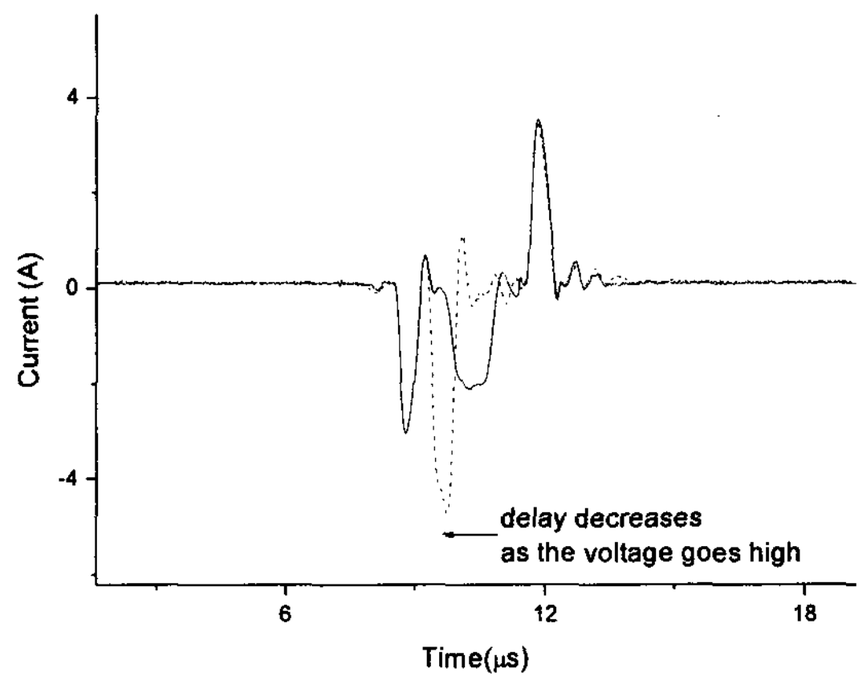

Fig. 5 Change of the discharge current when the address voltage is changed

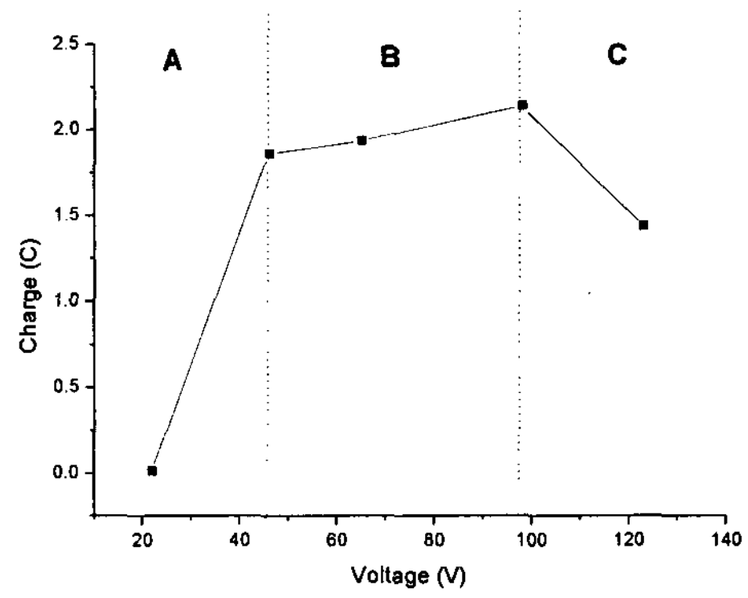

Fig. 6 The change of the amount of charge-flow during applying scan pulse in the address period

References

[1] LARRY F. WEBER, KEVIN W. WARREN, W. E. Howard, "Quantitative Wall Voltage Characteristics of AC Plasma Displays", in *Proc.* 1986 SID. Vol. 27/3.

[2] Takashi Hashimoto et al., IDW'97, pp 571-574.