Characterization of Thin Film Transistor using Ta_2O_5 Gate Dielectric

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Abstract

In this study, to get the larger drain current of the device under the same operation condition as the conventional gate dielectric SiNx thin film transistor devices, we introduced new gate dielectric Ta_2O_5 thin film which has high dielectric constant (~25) and good electrical reliabilities. For the application for the TFT device, we fabricated the Ta_2O_5 gate dielectric TFT on the low-temperature-transformed polycrystalline silicon thin film using the self-aligned implantation processing technology for source/drain and gate doping. The Ta_2O_5 gate dielectric TFT showed better electrical performance than SiNx gate dielectric TFT because of the higher dielectric constant.

Introduction

With an improvement in the integration density technology of large scale integrated devices, remarkable developments have been achieved in flat panel display devices, such as active matrix liquid crystal displays (AMLCDs), plasma display pannel (PDP). When the scan line turn on for a few microsecond time in AMLCDs, the quick pixel charging by thin film transistor (TFT) in these devices should be made to gives us images we wanted. As the panel size becomes larger and the resolution becomes higher, the charging time becomes shorter. We can achieve this quick charging by channel current increase. So far, there have been studies on new gate dielectrics to increase the capacitance per unit area in addition to the carrier mobility improvement in channel region[1,2]. Presently as a conventional gate dielectrics, PECVD a-SiOx or a-SiNx are deposited. The Ta_2O_5 film has already been applied as a gate insulator material for devices such as TFT, COG with a metal-insulator semiconductor (MIS) and metal-insulator-metal (MIM) structure, hydrogen sensitive devices and the electroluminecesnt devices with Si_3N_4/Ta_2O_5 bilayer structure. This is due to its high dielectric constant (~25) and excellent dielectric properties. Other potential uses of the Ta_2O_5 film are both gate oxides, which can replace the thermally oxidized SiO_2, and impurity penetration barrier for further scaling-down metal oxide semiconductor field effect transistor (MOSFET) devices under a limited thermal budget[3]. A gate oxide with a double layer of Ta_2O_5 film/SiO_2 and W Gate electrode has already been suggested for next generation devices[4].

In this work, we fabricated TFT devices newly using Ta_2O_5 film as a gate dielectric and determined the electrical characteristics by comparing conventional TFT using SiNx film as a gate dielectric.

Device Fabrication

Figure 1 depicts a cross–sectional view of a poly-Si TFT fabricated. A thermally oxidized Si (100) wafer was used as a substrate. A 2000 Å-thick amorphous silicon was initially deposited at 550 ℃ by low pressure chemical vapor deposition using SiH_4, and then furnace annealed at 600 ℃ for 24h in N_2 ambient to recrystallize such silicon films for the improvement of electron channel mobility. After defining the active region, Ta_2O_5 or SiN_X dielectric were deposited as a 1000 Å-thick gate dielectric, respectively. Ta_2O_5 thin films were deposited in RF (13.56 MHz) plasma enhanced chemical vapor deposition (PECVD) apparatus. The $Ta(OC_2H_5)_5$ liquid source was kept at 115 ℃ and carried by

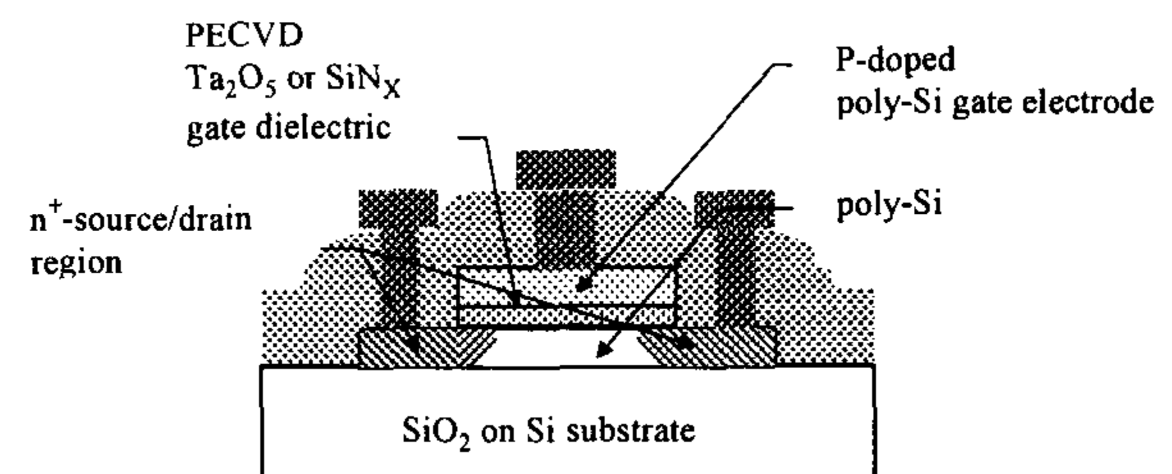

Fig.1. A cross-sectional view of a fabricated poly-Si TFT

Ar gas (250 sccm) into the reactor during deposition. The $Ta(OC_2H_5)_5$ delivery line was heated up to 140 ℃ to prevent vapor re-condensation. Pure N_2O gas (15 sccm) was used as an oxidant. Depositions were carried out at 0.45 Torr at 300 ℃. The RF power was 200 W. After deposition, N_2O plasma annealing was carried for 1h at 300 ℃, 200 W, 50 sccm of N_2O gas flow. Under these conditions, the relative dielectric constant of Ta_2O_5 thin film was found to be 22. On the other hand, SiN_X thin film was deposited at 300 ℃, 60 W using SiH_4/N_2 (800 sccm), N_2 (1200 sccm), NH_3 (10 sccm). Another 1500 Å-thick amorphous silicon was deposited at 550 ℃ in a LPCVD system and patterned as the gate area. A self-aligned P^+ ion implantation was performed at 60 Kev, $1.6*10^{16}$ cm^{-2} to dope source/drain and gate electrode. Additional annealing for dopant activation and polysilicon grain growth was performed at 600 ℃ for 4 h in N_2 ambient. After a plasma enhanced CVD TEOS with a thickness of about 5000 Å was deposited, the contact hole were opened and the Al containing 1 % Si films were sputtered and patterned. Finally, the alloying was done at 450 ℃ for 30 min in N_2 ambient to reduce the contact resistance.

Results and Discussion

Figure 1 shows the cross-sectional poly-Si TFT fabricated. The poly-Si TFTs with SiNx film as a gate dielectric were also fabricated for comparison.

The I_D vs V_D characteristics of the Ta_2O_5 gate dielectric TFT, shown in Fig.2, are similar to the typical MOSFET. But the drain current of the Ta_2O_5 gate dielectric TFT was much larger than a-SiNx gate dielectric TFT. The drain current is determined by C_{ox} of the gate dielectric of the device, which is as follows:

$$I_D = \frac{W}{L} \mu C_{OX} \left(V_G - V_T - \frac{1}{2} V_D \right) V_D$$

where W and L are the line width and length of the device, μ is mobiiity of the electron, C_{ox} is the capacitance of the gate dielectric,

V_T is the threshold voltage. Since the di electric constant of Ta_2O_5 was much larger than that of a-SiNx, C_{ox} of the Ta_2O_5 gate dielectric TFT was much larger. Thus, the devices with the Ta_2O_5 gate dielectric showed better drain current characteristics. We confirmed that low voltage operation could be possible by using Ta_2O_5 gate dielectric.

Figure 3 shows the transconductance and transfer characteristics of the poly-Si TFT at V_D=1V. The on/off current ratios obtained from the transfer curve were both ~10^5, but the transconductance of Ta_2O_5 gate dielectric TFT was 2.5 times larger than that of SiNx gate dielectric TFT. Also, the subthreshold slope was 0.9 V/dec for Ta_2O_5 gate dielectric TFT, compared to 1.6 V/dec for SiNx gate dielectric TFT. The fabricated Ta_2O_5 gate dielectric TFT exhibited a field effect mobility of 35~37 ㎠/Vs, shown in Fig.4, while SiNx gate dielectric TFT ~25 ㎠/Vs. The field effect mobility was obtained from the transconductance in the linear region at V_D=1V, i.e.,

$$g_m = \partial I_D / \partial V_G = C_i V_D \mu W / L$$

where W/L is the ratio of the channel width to channel length.

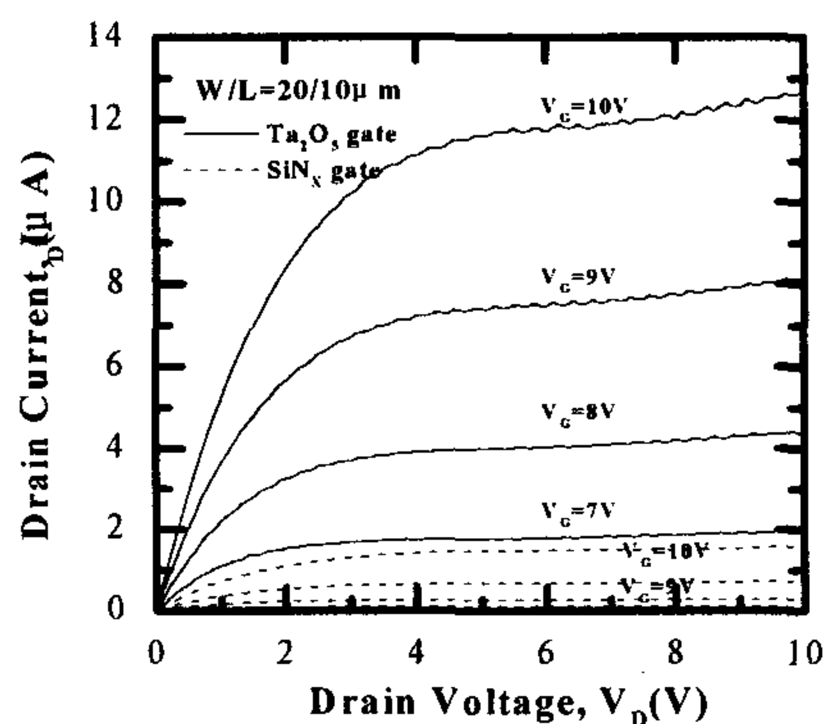

Fig.2. Room temperature drain-source current (I_D) versus drain-source voltage (V_D) characteristics for various gate biases V_G of TFT using Ta_2O_5 gate dielectric and SiNx gate dielectric

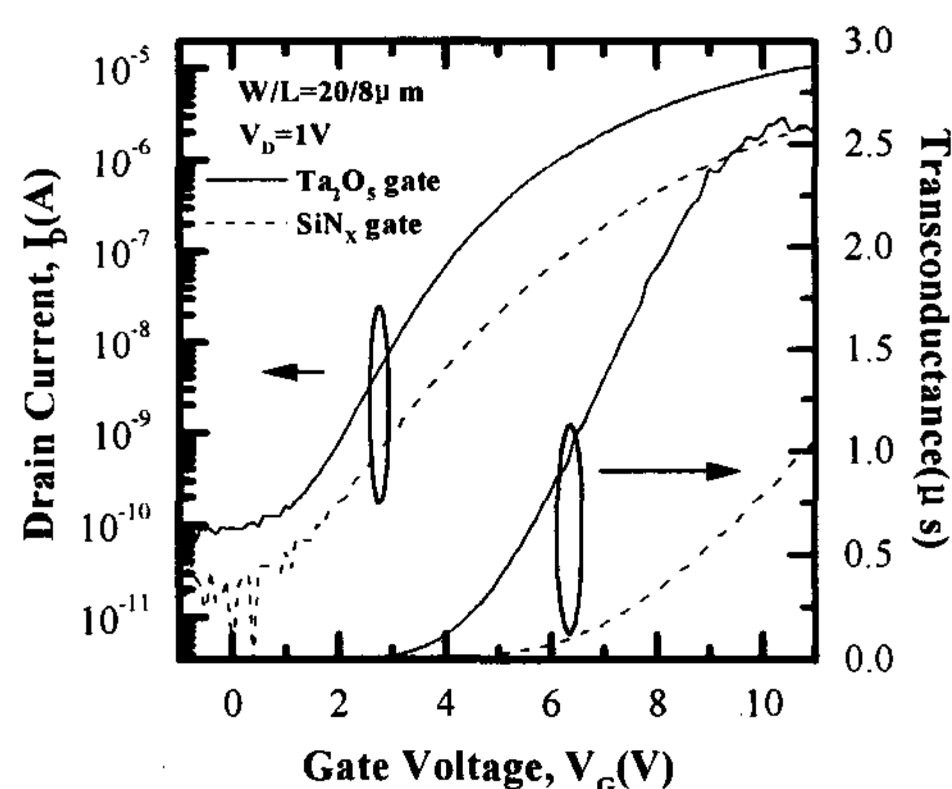

Fig.3. Room temperature transconductance and transfer characteristics of the fabricated poy-Si TFT at V_D=1V using Ta_2O_5 gate dielectric and SiNx gate dielectric

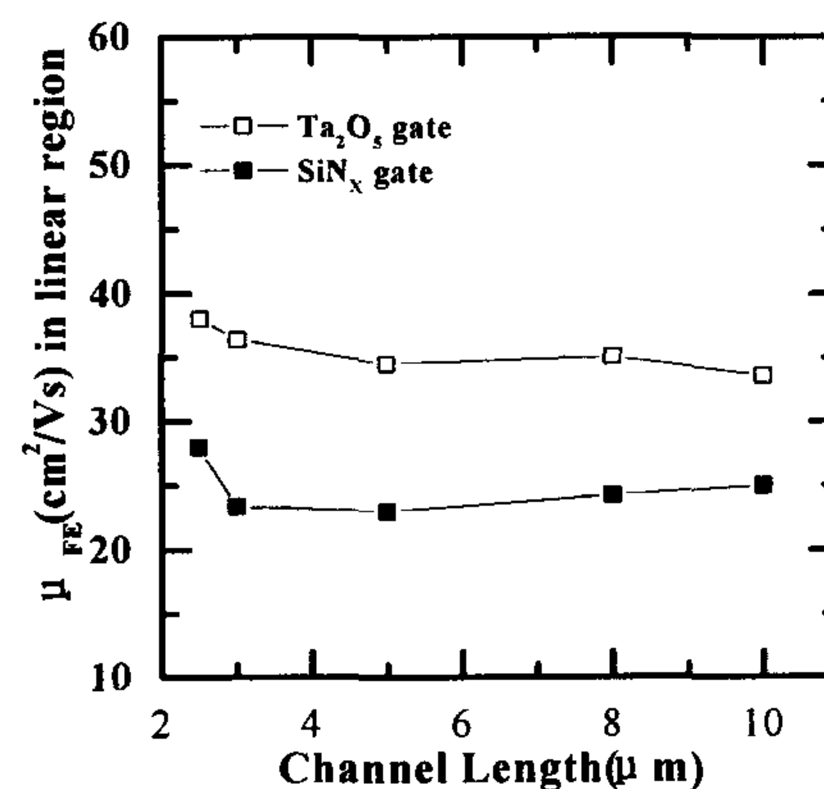

Fig.4. The variation of field effect mobility as a function of channel length of the fabricated poy-Si TFT using Ta_2O_5 gate dielectric and SiNx gate dielectric

Conclusion

We proposed a Ta_2O_5 gate dielectric material for poly-Si TFTs because of high dielectric constant. Ta_2O_5 gate dielectric TFTs showed much better electrical characteristics than those made by conventional SiNx gate dielectric TFTs. The mobility was 35~37 ㎠/Vs without hydrogen passivation in case of Ta_2O_5 gate dielectric TFT.

References

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