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64M DRAM의 Defect 관련 STI(Shallow Trench Isolated) NMOSFET Hump 특성

Hump Characteristics of 64M DRAM STI(Shallow Trench Isolated) NMOSFETs Due to Defect

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Abstract

In 64M DRAM, sub-1/4m NMOSFETs with STI(Shallow Trench Isolation), anomalous hump phenomenon of subthreshold region, due to capped p-TEOS/SiN interlayer induced defect, is reported. The hump effect was significantly observed as channel length is reduced, which is completely different from previous reports. Channel Boron dopant redistribution due to the defect should be considered to improve hump characteristics besides consideration of STI corner shape and recess.

Key Wards(중요용어) : DRAM, STI, NMOSFET, Hump, Defect

1. Introduction

LOCOS has been the traditional choice for isolation between devices in past MOSFET technologies. However, STI has been challenged widely as a substitute for the LOCOS isolation. It eliminates the LOCOS birds beak and is fully planar with the Si surface. Inherent to this geometry are fringing gate fields that enhance carrier inversion within the Si corner at the isolation edge. As a result, there exists a parasitic transistor of low threshold voltage(Vt) in parallel with the main MOSFET channel region. N-channel MOSFET with this parallel corner device shows hump in subthreshold current characteristics which results in increase of standby leakage current. In this paper, anomalous hump phenomenon in subthreshold region, with capped p-TEOS/SiN interlayer induced defect, is reported. Furthermore, it is mentioned that a parasitic transistor can be formed under local boron channel depletion induced by defect in a short channel NMOSFET. This results in significant hump effect as channel length is reduced.

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2. Experimental

Fig.1 shows a schematic cross section of LDD NMOSFET with capped interlayers. The capped interlayers consist of a p-TEOS or HLD oxide of 500nm under a LPCVD SiN of 30nm, or only a HLD oxide of 500nm. In NMOSFET process, 40keV B ions with a dose of 3e12/cm2 were implanted a tilt-angle of 30 degrees for halo pocket. As(20keV, 3e14/cm2) and P(20keV, 2e13/cm2) ions for n- implant are

performed to reduce source/drain parasitic resistance and hot carrier effect, followed by formation of SiN sidewall spacer of 70nm. Gate oxide thickness is 6.7nm. In STI process, CVD oxide deposited to fill trenches, followed by densification. CMP was applied to planarize the CVD oxide. The trench angle is 74.5 degrees and depth is 350nm.

Fig.2 shows cross-sectional SEM micrograph of STI with a round corner and recess of about 20nm.

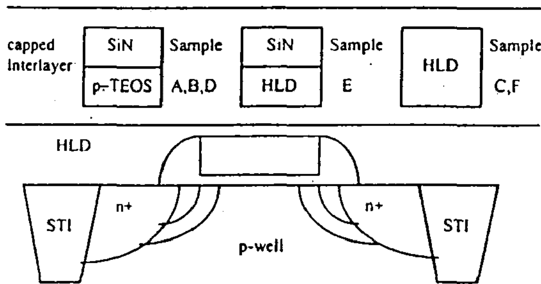

Fig. 1 Schematic diagrams of sample structures

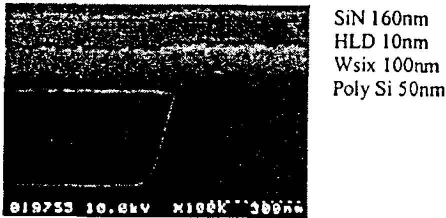

Fig 2 Cross-sectional SEM micrograph of STI profiles

3. Results and Discussion

Table1 shows NMOS process parameters of split samples. In Fig.3, hump effect of sample A which has capped layers of SiN/p-TEOS increases as channel length is reduced. This phenomenon is completely different from that reported by several authors[1,2] previously. It is well known that for short channel transistors, the hump effect almost disappears. This was due to the reduced sensitivity of the corner transistor to the short channel effect in comparison with that of the main transistor. For sample C

Table 1. NMOS Sample Parameters

Sample	A	B	C	D	E	F
Gate Oxide	SiO2	SiO2	SiO2	SiO2/NO	SiO2/NO	SiO2/NO
STI Recess	~20nm	~20nm	~20nm	~20nm	~20nm	~20nm
Channel (B^-, 20KeV)	2E12	1.4E13	2E12	4.6E12	4.6E12	4.6E12
Capped Interlayer	SiN/ p-TEOS	SiN/ p-TEOS	HLD/ HLD	SiN/ p-TEOS	SiN/ HLD	HLD/ HLD

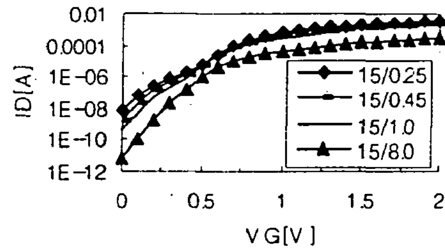

Fig. 3 Hump characteristics dependence on gate length of sample A

which has a capped interlayer of only HLD, any hump effects, regardless of channel length, are not shown in Fig.4. Carbon[3] defect due to the TEOS-based oxide under SiN and Hydrogen[4] defect due to the SiN capping layer have been reported previously. These defects may diffuse to the gate channel edge of high oxide field near STI. Channel boron dopant diffusivity is proportional to the defect concentration, which results in B-depletion at gate edge locally. In long channel length, sufficient boron dopant is provided from center to the gate edge. This prevents generation of a local parasitic transistor of low Vt. In short channel length, there is not sufficient dopant in the channel center. The resulting local B-depletion[5] makes a parasitic transistor of low Vt and enhances Vt roll-off. In Fig.5, S-factor under strong back bias of sample A and C are compared with respect to the gate length. Sample A has more interface defects than those of sample C because S-factor under strong back bias is proportional to gate interface defect density. In Fig.6, sample A shows

significant Vt roll-off characteristics via weak reverse short effect in comparison of those of same channel dose of sample C. Vt(sat) was measured at a normalized drain current of 0.1nA*(W/L) at Vds=2.5V. For sample B, even under SiN/p-TEOS induced defect, hump characteristics are not shown owing to the high channel dose in Fig.7. In Fig.8, hump effect is most significant in the sample D and not shown in sample F which has only the HLD interlayer.

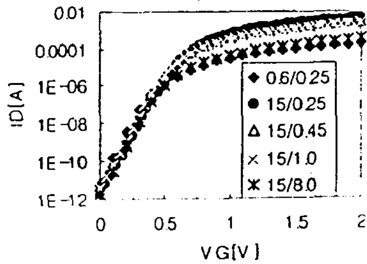

Fig. 4 Id-Vg characteristics of sample C with different Lg/W

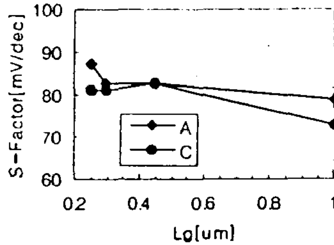

Fig. 5 S-factor(V_{bs}=-5V) vs. gate length of sample A and C

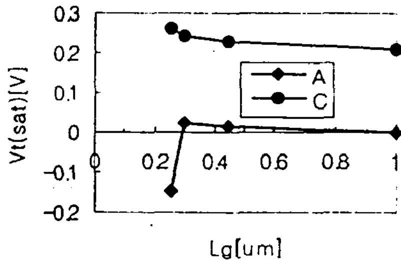

Fig. 6 Vt(sat) roll-off characteristics of sample A and C

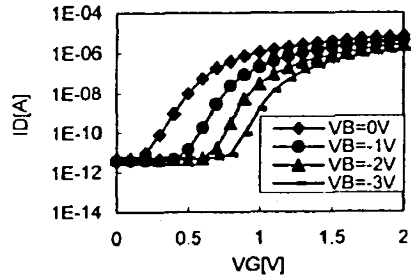

Fig. 7 Id-Vg characteristics of sample B

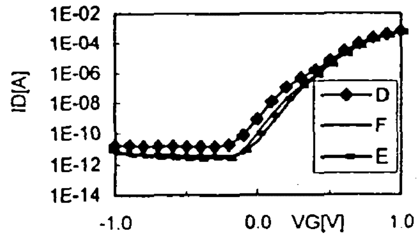

Fig. 8 Id-Vg characteristics of sample D, E and F

4. Conclusion

Interlayer, p-TEOS/SiN induced defect may diffuse to gate channel edge of high field near STI and make local boron channel depletion. This results in a parasitic transistor of low Vt and enhances Vt roll-off. Significant hump effect was observed as channel length is reduced, which is completely different from previous reports. In submicron Shallow Trench Isolated-NMOSFET of DRAM, channel dopant redistribution due to defect should be considered to improve hump characteristics besides STI corner shape and recess.

References

1. P. Sallagoity, M. Ada-Hanifi, M. Paoli, and M.Haond:IEEE ED. Vol.43, No.11 (1996) p.1900
2. P.J. VanDerVoorn and J.P. Krusius: IEEE ED. Vol.43, No.8 (1996) p.1274
3. H. Mori, et al: SSDM (1994) p.904
4. Richard B. Fair and Robert C. Sun: IEEE ED Vol.28, No.1 (1981) p.83
5. D.K.Sadana, A. Acovic, et al.: IEDM (1992) p.849