A High-Efficiency High-Power Step-Up Converter with Low Ripple Content

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Abstract–A new phase-shifted parallel-input/series-output (PISO) dual inductor-fed push-pull converter for high-power step-up applications is proposed. This converter is operated at a constant duty cycle and employs an auxiliary circuit to control the output voltage with a phase-shift between the two modules. It features a voltage conversion characteristic which is linear to changes in the control input, and high step-up ratio with a greatly reduced switch turn-off stress resulting in a significant increase in the converter efficiency. It also shows a low ripple content and low root-mean-square (RMS) current in the output capacitor. The operational principle is analyzed and a comparative analysis with the conventional pulse-width-modulated (PWM) PISO dual inductor-fed push-pull converter is presented. A 50kHz, 800W, 350Vdc prototype with an input of 20-32Vdc has also been constructed to validate the proposed converter. The proposed converter compares favorably with the conventional counterpart and is considered well suited to high-power step-up applications.

Key Words–DC/DC power converter, Step-up converter, High power, High efficiency, Low ripple

I. INTRODUCTION

Many applications require the step-up power converters to convert the low source voltage to a higher output voltage. In a distributed power system, for example, the front-end converter is required to convert the relatively low output voltage of the preceding stage for the power factor correction to a higher dc bus voltage in order to reduce the power distribution loss [1]. Here applies the step-up power conversion technique and the power demands are ever increasing. The fuel cell system makes another good application of the high-power step-up converter since the output voltage generated by each fuel cell is a relatively low value about 0.75V [2]. [3].

However, the development of a step-up power converter, particularly with high power capability, is difficult due to the problem of high input current, since it causes a serious degradation in the power conversion efficiency and step-up ratio [4], [5]. It sometimes results in an impracticably high switch current stress. Besides, the filter capacitor which in general has a large value to remove effectively the large ripple of the output voltage is also a problem.

In this paper, a new phase-shifted parallel-input/series-output (PISO) dual inductor-fed push-pull converter for high-power step-up applications is proposed. The circuit diagram of the proposed converter is shown in Fig. 1. This converter employs two dual inductor-fed push-pull converter modules [6] and an auxiliary circuit placed between the output stages of both modules. The dual inductor-fed push-pull converter, which is hereafter named in short as dual converter, is employed to take advantage of its high voltage conversion ratio and low device stress [7]. The PISO configuration [8] is adopted because the manner in which the current and voltage stresses are shared among modules is in favor of high-power step-up applications.

The proposed converter is operated at a constant duty cycle, and the auxiliary circuit produces an output voltage which is proportional to the phase-shift between the two modules. Due to this operational characteristic, this converter features low input current and output voltage ripples, and a constant switch voltage stress which is lower than that of the conventional PWM PISO dual converter. The switching loss developed during switching transients, therefore, is low in the proposed converter. Moreover, switching devices with lower voltage ratings, which generally have smaller turn-on impedance, can be used to achieve a further increase in the efficiency.

In the rest of this paper, the operation of the proposed converter is analyzed and a comparative analysis with the conventional PWM PISO dual converter is presented to discuss various features of the proposed converter. Also, experimental results from a 50kHz, 800W, 350Vdc prototype with an input voltage range of 20-32Vdc are presented to confirm the validity of the proposed converter.

II. OPERATIONAL PRINCIPLES

Fig. 1 shows a circuit diagram of the proposed converter. It consists of two identical dual converters with a common voltage source V_i, and an auxiliary circuit, which is composed of tertiary windings, a full-wave rectifier, and LC filter components. Both modules are operated at a constant duty cycle D with a phase-shift ϕ between the modules. The switching period is defined as T_s. To simplify the analysis, all the circuit components are assumed to be ideal. Also, all the inductors and the capacitors are assumed to be large enough to be approximated by constant current and voltage sources within one switching cycle.

The turns ratio of the primary and secondary windings is defined as $N = N_s/N_p$, and that of the primary and tertiary

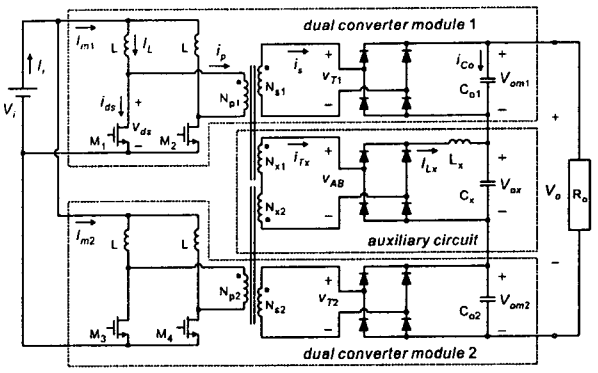


Fig. 1 Circuit diagram of proposed converter

windings is defined as $n = N_x/N_p$. The undotted ends of the tertiary windings are connected together so that the voltage between the dotted ends, denoted by v_{AB}, becomes $(n/N)(v_{T1} - v_{T2})$, where v_{T1} and v_{T2} are the instantaneous transformer secondary voltages. The voltage v_{AB} is rectified by the full-wave rectifier in the auxiliary circuit, and the LC filter produces an averaged dc voltage V_{ox}. Note that the dual converter has two operating phases: boost phase and powering phase. When both switches are turned on, the dual converter is said to be in a boost phase. When one of the switches is turned off, the dual converter is said to be in a powering phase. The boost phase continues for $(D - 0.5)T_s$ and the powering phase for $(1 - D)T_s$. By imposing the constant volt-second relationship on the boost inductor L, it is easily shown that the output voltage of each module is independent of ϕ, and is the same as that of a stand-alone dual converter, that is, $V_{om1} = V_{om2} = V_{om} = NV_i/(1 - D)$.

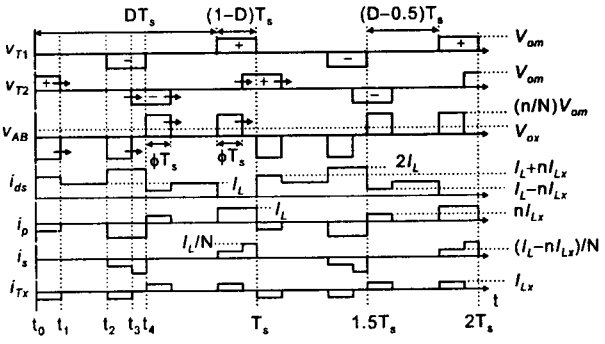
Key operating waveforms of the proposed converter are shown in Fig. 2 where the bottom module, denoted by module 2 in Fig. 1, is assumed to have a lagging phase. Waveforms of other switches and windings omitted in the figure can be obtained by shifting or mirroring their counterparts shown in Fig. 2. If $\phi = 0$, the waveforms of v_{T1} and v_{T2} completely overlap with each other. In this case, v_{AB} and the auxiliary output voltage V_{ox} become zero. If $\phi \neq 0$, the waveforms of v_{T1} and v_{T2} cannot be completely cancelled. The rectangular pulses of v_{AB} correspond to the non-overlapped portions of the waveforms of v_{T1} and v_{T2}. The LC filter in the auxiliary circuit averages $|v_{AB}|$ yielding V_{ox}, which is proportional to ϕ, as follows:

$$V_{ox} = 4\frac{n}{N}\phi V_{om}. \tag{1}$$

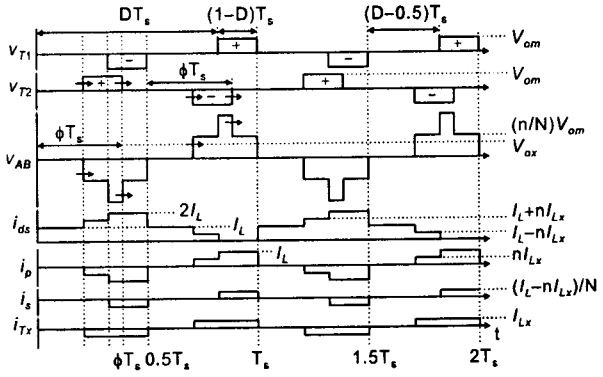
The current i_{Tx}, carried by N_{x1} and N_{x2}, has a similar waveform to v_{AB} with an amplitude equal to the current in L_x denoted by I_{Lx}. When $i_{Tx} \neq 0$, the current i_{Tx} is reflected to the primary of the module in a boost phase and circulates through the switching devices. On the other hand, in the module in a powering phase, the primary current flowing toward the secondary is shared with i_{Tx}. For example, from t_0~t_1 in Fig. 2(a), module 1 is in a boost phase and module 2 is in a powering phase. The tertiary current i_{Tx} which is equal to $-i_{Lx}$, is reflected to the primary of module 1 and circulates through M_1 and M_2, resulting in i_{ds}, the current in M_1, equal to $I_L + nI_{Lx}$. On the other hand, from t_2~t_3 in Fig. 2(a), module 1 is in a powering phase and module 2 is in a boost phase. The current i_{Tx} shares the primary current of module 1 flowing toward the secondary side, denoted by i_p, yielding the secondary current in module 1 $i_s = -(I_L - nI_{Lx})/N$. Therefore, the switch, primary, and secondary current waveforms shown in Fig. 2 are obtained.

If ϕ reaches $1 - D$, the rectangular pulses of v_{T2} entirely deviates from the equally signed pulses of v_{T1}. Therefore, those waveforms of v_{T1} and v_{T2} cannot be cancelled any more. Instead, all the pulses of v_{T1} and v_{T2} are individually reflected to the auxiliary circuit side. As ϕ is increased, the rectangular pulse of v_{T2} approaches the oppositely signed pulse of v_{T1} without affecting V_{ox}.

If $\phi = D - 0.5$, the rectangular pulse of v_{T2} meets the



(a) $\phi < 1 - D$



(b) $\phi > D - 0.5$

Fig. 2 Key waveforms of proposed converter

oppositely signed pulse of v_{T1} on the time axis, while the equally signed pulses of v_{AB} come together to match each other. If ϕ is further increased, overlapped portions of the oppositely signed pulses of v_{T1} and v_{T2} begin to appear, resulting in a stepwise waveform of v_{AB} as shown in Fig. 2(b). During this overlapping interval of the oppositely signed pulses of v_{T1} and v_{T2}, both modules are in powering phases with opposite polarities in the transformers. The voltages on N_{x1} and N_{x2} also have opposite signs, and the auxiliary circuit delivers power to the output with $v_{AB} = -2(n/N)V_{om}$. Although the waveshape of v_{AB} is modified as ϕ is increased, the total area of the waveform of v_{AB}, which is equivalent to V_{ox}, still remains independent of ϕ. Therefore, equation (1) can be generalized as

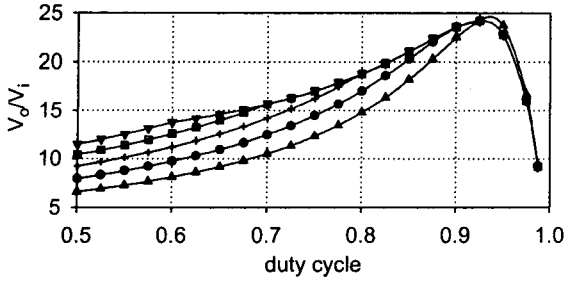
$$V_{ox} = 4\frac{n}{N}V_{om}\min\{\phi, 1-D\}. \tag{2}$$

The overall output voltage V_o of the proposed converter is equal to sum of V_{ox} and $2V_{om}$.

III. FEATURES AND COMPARATIVE ANALYSIS

A. Steady-state Voltage Conversion Characteristic

A duty cycle controlled step-up converter is generally considered to have an asymptotic voltage conversion characteristic, while a step-down converter has a linear one. The rapidly changing output voltage of the step-up



(▲: $\phi = 0$, ●: $\phi = 0.1$, ✚: $\phi = 0.2$, ■: $\phi = 0.3$, ▼: $\phi = 0.4$)

Fig. 3 Voltage conversion characteristic of proposed converter

converter makes a design of the feedback loop critical. Since the auxiliary circuit of the proposed converter makes an equivalent circuit of a step-down converter supplementing the constant outputs of both modules, the proposed converter has a voltage conversion characteristic which is linear and less sensitive to changes in the control input ϕ. The overall step-up ratio of the proposed converter, including the switch turn-on resistance, can be obtained as follows:

$$\frac{V_o}{V_i} = \frac{2N + 4n\phi}{1-D}\left[1 + \left\{8n^2\bar{\phi} + (3-2D)\left(\frac{N+2n\phi}{1-D}\right)^2\right\}\frac{R_{ds}}{R_o}\right]^{-1} \quad (3)$$

where $0 < \phi < 1 - D$ and $\bar{\phi} = \min\{\phi, D - 0.5\}$. The step-up ratio of the conventional PISO dual converter can be obtained by replacing ϕ in (3) with 0 as follows:

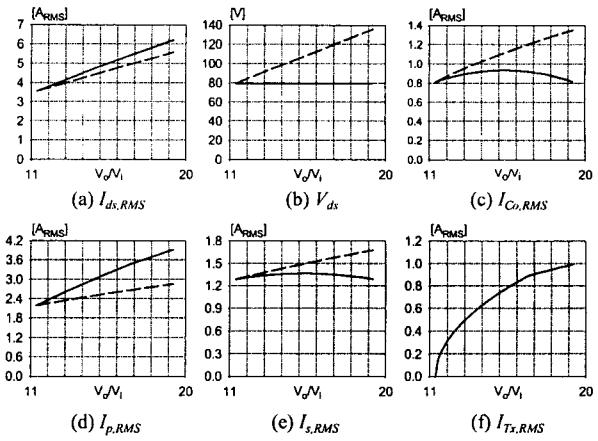
$$\frac{V_o}{V_i} = \frac{2N}{1-D}\left[1 + \left\{(3-2D)\left(\frac{N}{1-D}\right)^2\right\}\frac{R_{ds}}{R_o}\right]^{-1}. \quad (4)$$

The step-up ratios of the proposed converter for several different ϕ's are graphically illustrated in Fig. 3, where the transformer windings are designed as $N = 1.7$ and $n = 2$, and R_{ds} is assumed to be $0.0015R_o$. Note that the bottom curve, marked by upright triangles, represents the step-up ratio of the proposed converter when $\phi = 0$, which coincides with that of the conventional PISO dual converter given by (3). The other four curves in the figure show that, at the same duty cycle, the proposed converter gives a higher step-up ratio than the conventional PISO dual converter. To attain the same step-up ratio, the conventional PISO dual converter should be operated at a larger duty cycle than the proposed converter.

B. Device Stresses

Table I summarizes several important design equations of the proposed converter, where the phase-shift ϕ is assumed to be varied between 0 and $1 - D$. By matching the ampere-second balance of the output capacitor, the steady-state relation between I_o and I_L is obtained as follows:

$$I_L = \frac{N + 2n\phi}{2(1-D)} I_o \quad (5)$$



(—: proposed converter, ---: conventional PWM counterpart)

Fig. 4 Various device stresses of both converters

which is similar to the relation between V_o and V_i. Each equation of the RMS current can be normalized with respect to either I_L or I_o using (5). It is noted that the equations of the proposed converter are reduced to those of the conventional PISO dual converter by replacing ϕ with 0.

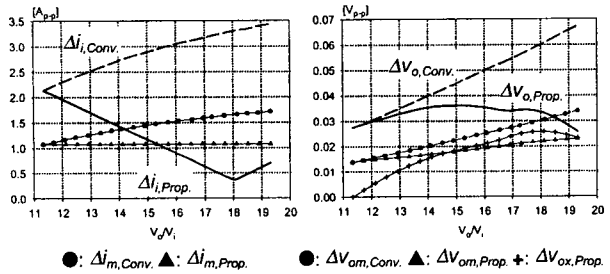
The equations in Table I are graphically illustrated in Fig. 4 as a function of step-up ratio, where all the RMS currents are normalized with respect to the load current I_o. The dashed line in each graph represents the stress in the conventional PISO dual converter obtained by varying D from 0.7 to 0.82. On the other hand, the solid line represents the stress in the proposed converter obtained by varying ϕ from 0 to 0.3 at $D = 0.7$. The transformer parameters are $N = 1.7$ and $n = 2$ as previously designed and the input voltage is $V_i = 24$Vdc.

Since the proposed converter is operated at a smaller duty cycle than the conventional PISO dual converter, it shows a somewhat larger switch RMS current than the conventional PISO dual converter. However, the smaller duty cycle of the proposed converter maintains the switch turn-off voltage V_{ds} constant, which is lower than that of the conventional PISO dual converter. It should be noted that a switching device with a lower voltage rating generally shows a lower conduction loss. The low switch turn-off

TABLE I
DESIGN EQUATIONS OF PROPOSED CONVERTER

Switch RMS current, $I_{ds,RMS}$	$\sqrt{2\bar{\phi}(nI_o)^2 + (3-2D)I_L^2}$
Switch turn-off voltage, V_{ds}	$\frac{V_i}{1-D}\left[1 + (3-2D)\left(\frac{N+2n\phi}{1-D}\right)^2\left(1 + 8n^2\bar{\phi}\frac{R_{ds}}{R_o}\right)^{-1}\frac{R_{ds}}{R_o}\right]^{-1}$
Output capacitor RMS current, $I_{Co,RMS}$	$\sqrt{(2D-1)I_o^2 + 2\phi\left(\frac{I_L - nI_o}{N} - I_o\right)^2 + 2(1-D-\phi)\left(\frac{I_L}{N} - I_o\right)^2}$
Primary RMS current, $I_{p,RMS}$	$\sqrt{2\bar{\phi}(nI_o)^2 + 2(1-D)I_L^2}$
Secondary RMS current, $I_{s,RMS}$	$\frac{1}{N}\sqrt{2\phi(I_L - nI_o)^2 + 2(1-D-\phi)I_L^2}$
Tertiary RMS current, $I_{Tx,RMS}$	$I_o\sqrt{2(\phi + \bar{\phi})}$

* Each expression can be normalized with I_o or I_L using (5).



(a) Input current ripple, Δi_i (b) Output voltage ripple, Δv_o

Fig. 5 Theoretical input current and output voltage ripples of both converters

voltage of the proposed converter therefore reduces not only the switching loss but also the conduction loss by using a switching device with a smaller R_{ds}. It is shown in Figs. 4(a) and (b) that the proposed converter shows a maximum 40% lower switch turn-off voltage than the conventional PISO dual converter at the expense of only 10% increase in the switch RMS current. Since the conventional PISO dual converter shows a maximum V_{ds} of 135V, IRFP250 with the voltage rating BV_{dss} of 200V and R_{ds} of 0.085Ω would be a good choice provided that a proper snubber circuit is employed. On the other hand, the proposed converter shows a constant V_{ds} of 80V over the entire operation range, so that IRFP150 with BV_{dss} of 100V and R_{ds} of 0.055Ω can be used to improve the efficiency.

Fig. 4(c) shows that the output capacitor RMS current is small in the proposed converter. This advantage facilitates the selection of the high voltage output capacitor of the proposed converter. Figs. 4(d), (e), and (f) show the RMS currents in the transformer windings of both converters. The secondary current is somewhat larger in the conventional PISO dual converter, while the primary RMS current is somewhat larger in the proposed converter.

C. Input current and output voltage ripples

It is obvious that the peak-to-peak input current ripple of the proposed converter is considerably reduced by the phase-shifted operation. The phase-shifted operation together with a phase-delay in the *LC* filter also results in a low peak-to-peak output voltage ripple by making all three ripple components of the proposed converter, which are Δv_{om1}, Δv_{om2}, and Δv_{ox}, out of phase with one another. Assuming a resistive load R_o = 150Ω and an input voltage V_i = 24Vdc, the ripple contents of both converters are numerically evaluated. The results are shown in Fig. 5. The converter parameters are C_o = 600μF, C_x = 100μF, L = 180μH, L_x = 140μH, N = 1.7, n = 2, and f_s = 50kHz. Note that the capacitor C_x in the auxiliary circuit is designed to be quite smaller than C_o since the *LC* filter is more effective than a pure *C* filter in removing switching ripples.

Fig. 5(a) illustrates the input current ripples of both converters, which are denoted by $\Delta I_{i,Conv.}$ and $\Delta I_{i,Prop.}$, and their ripple components from the individual modules as a function of step-up ratio. The low overall input current ripple of the proposed converter reduces the required size of the filter capacitor at the converter input. Fig. 5(b) shows that the auxiliary circuit of the proposed converter itself

TABLE II
CIRCUIT PARAMETERS OF PROPOSED CONVERTER

Switching frequency (f_s)	50 (kHz)
Switching devices (M_1, M_2, M_3, and M_4)	IRFP150
Boost inductor (L)	180 (μH)
Dual convertor output capacitor (C_o)	600 (μF)
Auxiliary circuit inductor (L_x)	140 (μH)
Auxiliary circuit capacitor (C_x)	100 (μF)
Turn ratio of secondary : primary (N)	1.7
Turn ratio of tertiary : primary (n)	2

produces as large a voltage ripple as the ripple of the individual module. However, due to the phase differences, the proposed converter shows a still lower overall voltage ripple than the conventional PISO dual converter in spite of the additional ripple component Δv_{ox}.

IV. EXPERIMENTAL RESULTS

A 50kHz, 800W, 350Vdc prototype with an input voltage range of 20-32Vdc has been constructed with circuit parameters shown in Table II. The rated input is 24Vdc and the rated operating conditions are D = 0.7 and ϕ = 0.15. The switches are driven at a constant duty cycle and a phase-shift is employed to control the output voltage. The conventional PISO dual converter is realized with the same components to those of the proposed converter except that the switching devices are IRFP250 due to the higher switch turn-off stress. The rated operating condition of the conventional PISO dual converter is D = 0.78.

Fig. 6(a) shows the experimental operating waveforms of the proposed converter at the rated conditions, where RCD snubbers are employed to protect the switches from high voltage surges. The waveforms clearly verify the theoretical operating waveforms shown in Fig. 2(a). Fig. 6(b) shows another results for D = 0.7 and ϕ = 0.4 with a reduced input voltage. In this case, the phase-shift is so large that the overlap of oppositely signed waves of v_{T1} and v_{T2} takes place. These waveforms correspond to Fig. 2(b).

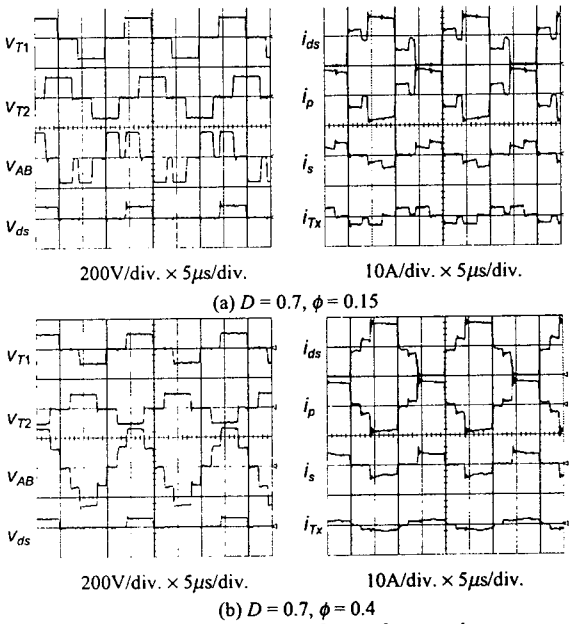
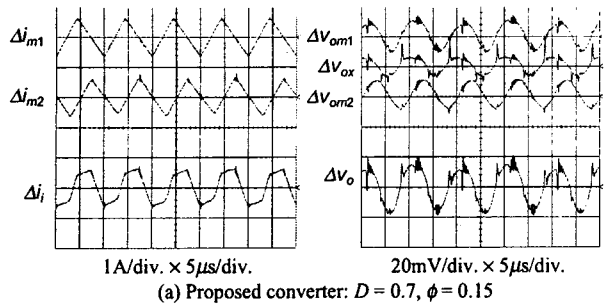
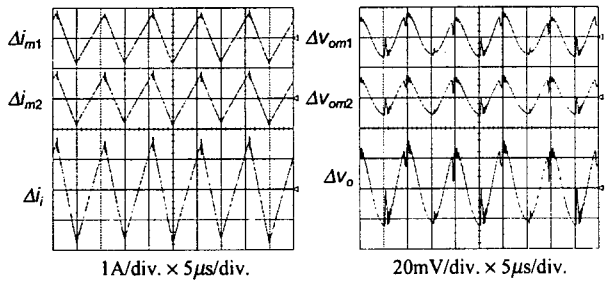


Fig. 6 Experimental operating waveforms of proposed converter



(a) Proposed converter: $D = 0.7$, $\phi = 0.15$



(b) Conventional PISO dual converter: $D = 0.78$

Fig. 7 Experimental ripple waveforms of both converters

Fig. 7 shows the experimental waveforms of the input current and output voltage ripples of both converters. To enhance the visibility, high frequency noises are smoothed by averaging the waveforms. It is clearly demonstrated that the phase-shifted operation partially cancels the individual ripple components to result in a low overall ripple. It is also shown that output voltage ripple of the proposed converter is small in spite of the additional ripple component introduced by the auxiliary circuit.

Fig. 8 shows the measured efficiencies of both converters. The solid line represents the efficiency of the proposed converter with IRFP150 and the dashed line represents the efficiency of the conventional PISO dual converter with IRFP250. The dotted line shows another result obtained from the proposed converter with IRFP250. As IRFP150 has a smaller turn-on resistance than IFRP250, the proposed converter, of course, has a higher efficiency. Furthermore, the dotted line shows that the proposed converter still has a higher efficiency than the conventional PISO dual converter, although both converters make use of the same switching devices. This is because the low switch turn-off voltage of the proposed converter results in a low switching loss developed during switching transients.

V. CONCLUSIONS

A new phase-shifted parallel-input/series-output dual inductor-fed push-pull converter based on a conventional two-module PISO modular dual inductor-fed push-pull converter is proposed. Both modules are operated at a constant duty cycle and the output voltage is controlled with a phase-shift between two modules. The operation principle of the proposed converter is analyzed and its features are discussed in comparison with the conventional two-module PISO dual converter. Also, experimental results from a 50kHz, 800W, 350Vdc prototype with an input voltage range of 20-32Vdc are presented to validate

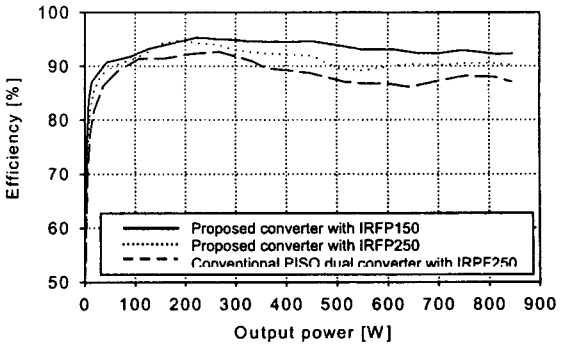


Fig. 8 Experimentally measured efficiencies of both converters

the proposed converter. The proposed converter compares favorably with the conventional PISO dual converter in many aspects as described below.

The proposed converter shows a high step-up ratio with a greatly reduced switch turn-off stress, so that it is possible to use a switching device with a low turn-on loss. The low switch turn-off voltage also reduces the switching loss developed during switching transients. These compromise the slightly increased switch RMS current and result in a significant improvement in the power conversion efficiency. Moreover, the proposed converter shows a small RMS current in the output capacitor and low input current and output voltage ripples. Since the proposed converter shows a voltage conversion characteristic which is linear to control input variations, it can be more easily stabilized. Therefore, the proposed converter is considered to be well suited to high-power and high-output voltage applications.

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