Improvement of Boron Penetration and Reverse Short Channel Effect in 130nm W/WN_x/Poly-Si Dual Gate PMOSFET for High Performance Embedded DRAM

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ABSTRACT

This paper presents the improvement of the boron penetration and the reverse short channel effect (RSCE) in the 130nm W/WN_x/Poly-Si dual gate PMOSFET for a high performance embedded DRAM. In order to suppress the boron penetration, we studied a range in the process heat budget. It has shown that the process heat budget reduction results in suppression of the boron penetration. To suppress the RSCE, we experimented with the halo (large tilt implantation of the same type of impurities as those in the device well) implant condition near the source/drain. It has shown that the low angle of the halo implant results in the suppression of the RSCE. The experiment was supported from two-dimensional(2-D) simulation, TSUPREM4 and MEDICI.

I. INTRODUCTION

Recently, it was discussed that W/WN_x/Poly-Si dual gate concept was applied in the gate structure for the embedded DRAM process. In order to make the high performance and the high density embedded DRAM, the surface channel PMOSFET and the self-aligned-contact (SAC) scheme are the required process concept.

When the W/WN_x/Poly-Si surface channel PMOSFET is applied in the gate structure for the high performance embedded DRAM, we are faced with the boron penetration problem. The high doped boron atoms in the gate poly pass through the gate oxide to a transistor channel region by the followed heat budget process. This counter doping in the transistor channel causes a decrease in the threshold voltage.[1][2]

The deep sub-micron CMOS process for the high density embedded DRAM has a major problem, the Reverse Short Channel Effect (RSCE). The non-uniform doping with higher doping concentration near the source/drain regions will result in an increase in the average doping concentration in the channel and hence cause an increase in the threshold voltage.[3] As the device channel length becomes shorter, this non-uniform lateral doping profile may cause a significant increase in the threshold voltage. This is known as the RSCE. Generally, the halo (large tilt implantation of the same type of impurities as those in the device well), as a source/drain structure, is applied in the deep sub-micron devices. Doping of the halo has overlapped the doping of the channel, it causes an increase in the average doping concentration in the channel.

This study presents the improvement of the boron penetration and the RSCE in 130nm W/WN_x/Poly-Si dual gate PMOSFET for a high performance embedded DRAM. We concluded that the process heat budget reduced the results in suppression of the boron penetration and the low angle of the halo implant results in suppression of the RSCE.

II. EXPERIMENT

Our experiment was performed on the W/WN$_x$/Poly-Si dual gate PMOSFET, it was fabricated with the bulk CMOS process. The minimum gate length was about 130nm and the gate oxide thickness was about 1.2nm.

At first, a device well & shallow trench isolation (STI) was formed. The gate oxide was grown by the nitric oxidation method. A polysilicon was deposited by LPCVD. The boron was implanted into the polysilicon on the PMOSFET, followed by the rapid thermal anneal (RTA) process. WN and W was deposited by the ENDURA system, and then the gate was patterned. The arsenic was used for the p- halo implant and BF_2 was used for the p- source/drain extension implant. The p+ source/drain was doped with boron, followed by the rapid thermal anneal (RTA) process. Fig. 1 shows the W/WN$_x$/Poly-Si PMOSFET.

In order to confirm the boron penetration, we experimented with the range of the process heat budget. Test conditions are listed in Table. 1. To suppress the RSCE, we experimented with the p- halo implant condition near the source/drain. Test conditions are listed in Table. 2.

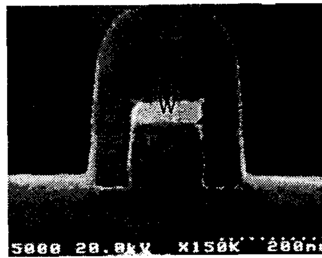

Figure. 1 W/WN$_x$/Poly-Si PMOSFET structure

Process	A	B	C	D
P+Poly RTA	skip	skip	950℃ 10sec	950℃ 10sec
P-Halo Implant (75As, 120keV)	2.4e13/40°			
P+S/D RTA (10초)	1000℃	1025℃	1000℃	1025℃

Table. 1 Test conditions for the suppression of the Boron penetration

Process	E	F	G	H
P+Poly RTA	skip			
P-Halo Implant (75As, 120keV)	1.3e13 30°	1.5e13 30°	1.5e13 40°	2.4e13 40°
P+S/D RTA	1000℃/ 10sec			

Table. 2 Test conditions for the suppression of the RSCE

The experiment was supported from two-dimensional(2-D) simulation, TSUPREM4 and MEDICI.[4] HP4062 semiconductor parametric analyzer system, as an electrical measurement equipment, has been chosen.

III. RESULTS & DISCUSSION

3.1 Boron penetration

Fig. 2 shows the doping concentration profile by the process simulation. An increase in the process heat budget caused an increase in the average doping concentration in the channel. It has shown that an increase in the process heat budget resulted in an increase in the boron penetration.

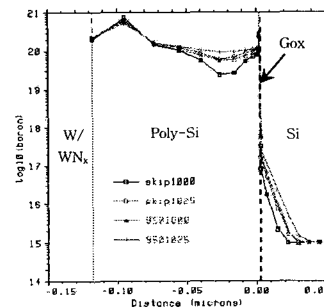

Fig. 2 The boron concentration profile by the process simulation

As an experiment result. Fig. 3 shows the relation between the threshold voltage and the process heat budget. The decreasing of threshold voltage was the most improved in group-A (p+ poly RTA skip, p+ S/D RTA 1000℃). It agrees well with the process simulation as shown in Fig. 2.

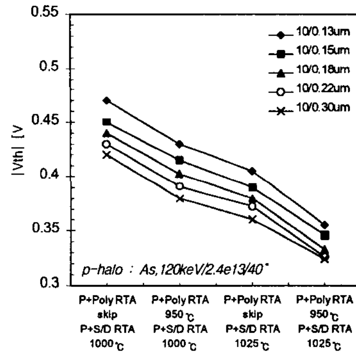

Fig. 3 PMOSFET Vth vs. the process heat budget

Fig. 4 shows that the suppression of the boron penetration causes a deepening of the RSCE.

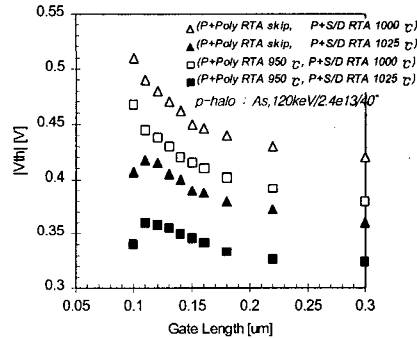

Fig. 4 PMOSFET Vth vs. Gate Length(@Width=10um)

3.2 Reverse short channel effect (RSCE)

To account for the lateral non-uniform doping effect due to the higher doping concentration near the drain and the source than in the middle of the channel, a step doping profile along the channel length direction as shown in Fig. 5 may be used as a first order approximation to obtain a V_{th} expression.[5]

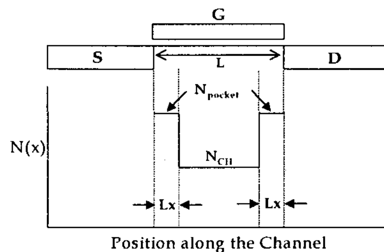

Fig.5 a step doping profile along the channel length direction

As a further approximation, the average channel doping can be calculated as follows[5]:

$$N_{eff} = \frac{N_{CH}(L-2L_x)+N_{pocket}\cdot 2L_x}{L} = N_{CH}\left(1+\frac{2L_x}{L}\frac{N_{pocket}-N_{CH}}{N_{CH}}\right) = N_{CH}\left(1+\frac{N_{LX}}{L}\right) \quad (1)$$

Where $N_{LX} = 2L_x\frac{N_{pocket}-N_{CH}}{N_{CH}}$.

N_{LX} is treated as a fitting parameter extracted from the measured data. With the introduction of N_{LX} to account for the lateral non-uniform doping, threshold voltage may be modified into

$$V_{th} = V_{TH0} + K_1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) - K_2 V_{bs} + K_1\left(\sqrt{1+\frac{N_{LX}}{L}}-1\right)\sqrt{\phi_s} \quad (2)$$

$(K_1, K_2 : \textit{Fitting parameter})$

Eq.(2) can best be understood by first setting V_{bs}=0. At V_{bs}=0, Eq.(2) models the dependence of threshold voltage on L_x due to the lateral non-uniform doping. Eq.(2) shows that the threshold voltage will increase as channel length decrease.[5] The p- halo implant conditions, a process parameter of N_{LX} ($\propto L_x$,N_{pocket}), were tested for the suppression of the RSCE.

Fig. 6 shows the relation between the threshold voltage of the PMOSFET and the p- halo implant conditions.

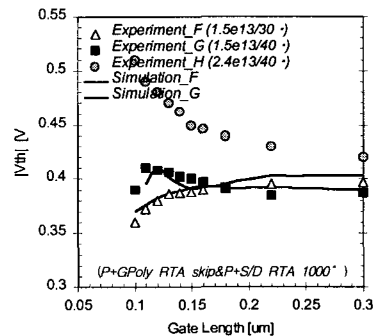

Fig. 6 PMOSFET Vth vs. p- halo implant condition(@Width=10um)

It has shown that group-F has a better characteristic for suppression of RSCE than group-G,H. As the low angle ion implant made a shift of a peak of doping concentration to the source/drain direction, it caused a decrease L_x and hence caused the average doping concentration (N_{eff}) in the short channel transistor. It has resulted in suppression of the RSCE. It agrees well with the device simulation (MEDICI).

Fig. 7 shows the relation between the ΔVth of the PMOSFET and the p- halo implant conditions. The group-E,F has a better characteristic for suppression of the RSCE than group-G,H. It has shown that the lower doped ($\approx N_{pocket}$) ion implant made little improvement of the ΔVth in the short channel transistor. In this experiment, for a suppression of the RSCE, it was important that we made a decision about a peak ($\approx L_x$) of doping concentration, as the angle of the p- halo implant, in a proper transistor structure and application.

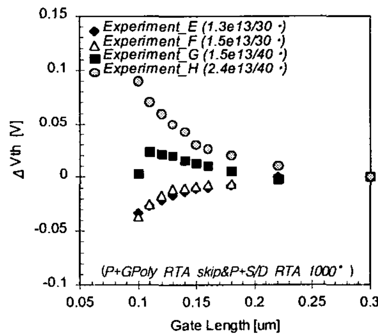

Fig.7 PMOSFET ΔVth vs. p-halo implant condition(@Width=10um)

3.3 Gate sheet resistance

In case of the W/WN_x/Poly-Si structure, gate sheet resistance was lower than W_{six}/Poly-Si structure as the gate structure of a conventional DRAM, it has shown in Fig. 8. The use of the W/WN_x/Poly-Si structure made a lower height of the gate because of the low sheet resistance in W. It has been an advantage of the inter-layer-dielectic (ILD) gap-fill for the self-aligned-contact (SAC) scheme in the high density embedded DRAM.

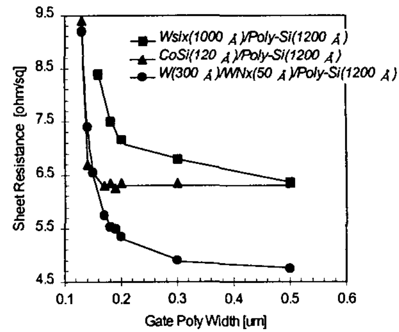

Fig. 8 Sheet resistance in gate structure

Ⅳ. CONCLUSION

In this experiment, we concluded that the boron penetration was reduced by the p+ poly RTA omission and the p+ source/drain RTA optimization.

Also, it has shown that the lower doped($\approx N_{pocket}$) ion implant made little improvement of the ΔVth in the short channel transistor. for a suppression of the RSCE. It was important that we made a decision about a peak ($\approx L_x$) of doping concentration, as the angle of the p- halo implant, in a proper transistor structure and application.

The use of the 130nm W/WN_x/Poly-Si dual gate PMOSFET structure made advantages for the high performance and the high density embedded DRAM.

Ⅴ. REFERENCE

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[4] TSUPREM4 and MEDICI Manuals.

[5] Yuhua Cheng & Chenming Hu, "MOSFET modeling & BSIM3 user's guide" *Kluwer Academic Publishers*, p.80-84, 1999.