A Family of Continuous Conduction Mode with Quasi Steady State Approach based on the General Pulse Width Modulator

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Abstract

This paper presents a family of continuous conduction mode with constant-switching pulse width modulator controllers. Unified implementation of quasi steady state approach for various DC-DC converters topologies is illustrated. The property and control low for quasi-state approach will be discussed in this paper. The different procedures will be discussed in details with different results for five commonly used DC-DC converters. Both trailing and leading edge pulse width modulation are used. Leading edge modulation can some times lead to simpler control circuitry as will be demonstrated in some circuits. These controllers do not require the multiplier in the voltage feed back loop, error amplifier in the current loop and rectified line voltage sensor, which are needed by traditional control methods. Controller examples and design are analyzed.

I. Introduction

A single phase diode followed by a DC-DC converter with a proper control method forms a rectifier with controlled dc-dc converter. The resister emulator is the rectifier which its impedance appears to be resistive in which the input voltage and the input current has the same shape. There are two traditional approaches to control a resister emulator namely, the voltage approach and the multiplier approach. The voltage-follower approach achieves resister emulator with the constant duty ratio or constant ON time control such as Cuk converter operating at DCM or a boost converter at the boundary of DCM and CCM. The control circuit is the simple voltage mode pulse width modulation (PWM) which dose not require current sensor. At high power applications, the current stress and current ripple become too large for a single DCM converter to operate efficiently. Therefore, the voltage-follower approach is not suitable for high-power application. Another approach is the multiplier approach which requires relatively complicated circuit. The control method is based on the current mode control. The components of this approach is shown on the figure below figure 1.

Comparing with the voltage follower approach, the multiplier approach operates in CCM so they are suitable for high power applications. The disadvantage of the multiplier approach is the large

current distortion due to the current ripple in the peak current mode control. Some methods applying to reduce the current distortion such as the using of current transformer as current sensor, but still there is additional current distortion result due to the non linearity of the of the multiplier New approach has been initiated for the resistor emulator. This new approach is named quasi steady state because it utilizes the property of the quasi steady state operation of the CCM converters to simplify the control circuitry.

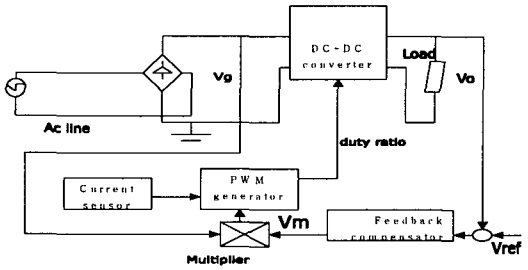

Figure 1. Multiplier approach controller

The circuit diagram on fig(2) shows this new approach. This paper will focus on the common property of the quasi stead state approach. The general PWM modulator will be reviewed briefly[1]. The unified quasi stead state approach for resistor emulator will be discussed at last section of this paper.

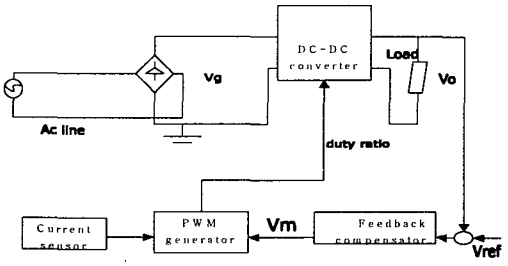

Figure 2. Circuit disgram

II. Quasi steady state approach

A quasi steady state occurs in the DC-DC converter when its input and load remain unchanged for a long time and the control law governing the converter is stable[2, 3]. The converter ties to converge to its steady state if the control law is stable. Even though the converter can never reach the true switching frequency steady state. All quantities in the quasi steady state operation can be approximated with their steady state value. The mean of resister emulator is to force the input current of the DC-DC converter to be proportional to the input voltage so that the input impedance is resistive. The local average at the input current can be obtained as follows :

$$\langle i_g \rangle = v_g / R_e \quad \text{..... (1)}$$

Where R_e is the emulate resistance, $\langle i_g \rangle$ controlled by the duty ratio. The control law is :

$$R_s * \langle i_g \rangle = v_m / M(d) \quad \text{..... (2)}$$

Where R_s is the equivalent sensing resistance, M(d) is the voltage conversion ration and v_m is the modulation voltage. As shown in the figure below. In the CCM DC-DC converter the steady duty ration D is :

$$V_o/v_g = M(D) \quad \text{..... (3)}$$

Where V_o is the output voltage. Substituting equ(3) into equ(2) yields to :

$R_s\langle i_g \rangle = v_m\, v_g/V_o$ =>Quasi steady state approximation

Where : v_m , V_o are constants ; $\langle i_g \rangle$ is proportional to v_g and the emulated resistance is :

$$R_e = R_s V_o / v_m.$$

Various implementations have been shown for the PWM modulator. These implementations can be unified with general PWM modulator.

III. The general PWM modulator

As shown in the fig(3) the general PWM modulator contains two stages of integrator with reset, flip flop, clock generator and a comparator. v_1, v_2, v_3 are control inputs. The output can be taken either from Q or Q'. The integrator has two cases. Case one when the reset value is low so the integrator will performs the normal Integration. Case two when the reset value is high so the integrator will reset to zero. The reset takes its value from Q'. When the voltage V(t) at the non inverting input of CMP reaches the voltage at the inverting input. CMP outputs a logical high signal resetting the flip flop and both integrators. The equations which define the general PWM modulators are :

$$v_t(t) = v_2(t/T_s) + v_3(t/T_s)^2$$

As we mention before we have two outputs for the PWM, which are Q, Q' so we can obtain two modul-a tion trailing modulation in which the leading-edge of Q pulse and leading-edge modulated in which the leading edge of Q' pulse When

$v_t = v_1$ so...

$v_1 = v_2\, d + v_3\, d^2$ .. (4)=>for the trailing modulation

$v_1 = v_2(1-d) + v_3(1-d^2)$ for the leading modulation.

In the next section we will drive v_1, v_2, v_3 for the various power topology using trailing edge modulation.

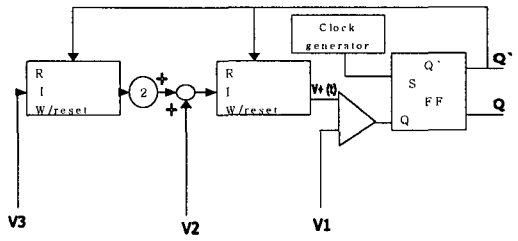

Figure 3. General PWM modulator

3.1 Unified implementation of quasi steady state approach

To demonstrate the derivation of v_1, v_2, v_3 we will use the boost and buck boost topologies as examples.

a) The boost converter topology

Fig(4) show the boost topology for the boost converter with the general PWM modulation. In the boost topology :

$$\langle i_g \rangle = \langle i_L \rangle \quad \text{..... (5)}$$

Substitute equ(5) into equ(2) yields with

$$M(d) = 1/(1-d)$$

$$R_s\langle i_L \rangle = v_m(1-d) \quad \text{..... (6)}$$

Using trailing edge modulation with its control in equ(4) arranging equ(6) yields to :

$$v_m - R_s\langle i_L \rangle = v_m d \quad \text{..... (7)}$$

Comparing equ(7) with equ(4) we can obtain the value of the control la law as :

$$v_1 = v_m - R_s\langle i_L \rangle \;;;;\; v_2 = v_m \text{ and } v_3 = 0$$

the above equation is called the control law of the average current m model control because the use of the average quantity. We can obtain the inductor-current controller for the trailing modulated boost topology by replacing the average inductor current with simpler instant current with a little assumption that the current ripple in the inductor is negligible. The average switch current control law can be found by integrating each term in equ(7) one more time. The average switch current $\langle i_T \rangle$ relates to the inductor current by

$$i_T > -di_L \quad \text{..... (8)}$$

for the boost converter, i_L from equ(8) into equ(7). Yields the fundamental control law for the NLC (None Linear Control)

$$R_s\langle i_T \rangle = v_m d - v_m d^2 \quad \text{..... (9)}$$

Comparing equ(9) with equ(4) we obtain the control value for v_1, v_2 and v_3 as :

$$v_1 = Rs\langle i_T \rangle \;;\; v_2 = v_m \;;\; v_3 = v_m.$$

In the other hand we can drive the control value for v_1, v_2, v_3 using leading edge modulator. For example equ(6) which indicates the control mode. Comparing this equation with leading edge equation (4-b) yields :

$$v_1 = R_s\langle i_L \rangle \;;\; v_2 = v_m \;;\; v_3 = 0$$

And assuming negligible current ripple same value can be obtain for the inductor-current control law. For the noise immunity reason we can use the average switch current sensor. Replacing i_L with :

$$i_L = \langle i_D \rangle/(1-d)$$

So,

$$R_s\langle i_D \rangle = v_m(1-d)^2$$

Table 1 shows three topologies with two modulation (trailing and leading) and three control laws for each modulation. As demonstrated in some controllers, the value of v_3 is equal to zero, there for only one stage of integrator is actually needed which simplified these controllers. The advantages of the leading edge over the trailing edge are :

1. The current sensing circuitry for some derived topologies with multiple switches is simplified.
2. The switching ripple current in output filtering capacitor can be reduced.

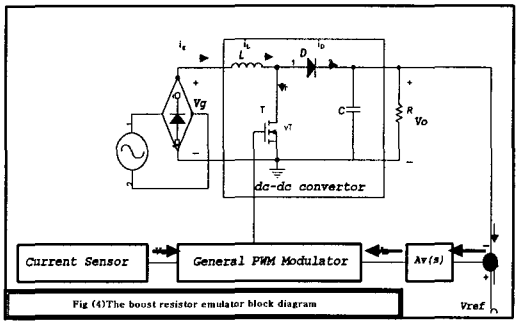

Figure 4. The boost resistor emulator block

b) The Buck-Boost converter topology

As shown in the fig(5) the buck-boost topology satisfies :

$$\langle i_g \rangle = \langle i_t \rangle \text{ and } M(d) = d/d\text{-}1$$

Using trailing edge modulation Replacing $\langle i_g \rangle$ in equ(2) with $\langle i_t \rangle$ we can obtain the average switch current control law :

$$V_m = (v_m + R_s\langle i_t \rangle)\, d$$

Comparing with trailing edge modulation equation :

$v_1 = v_m$; $v_2 = v_m + R_s\langle i_t \rangle$; $v_3 = 0$.

Also for the buck-boost converter

$$\langle i_t \rangle = di_L$$

So the inductor current law is :

$$v_m = v_m d + R_s * i_L * d_2$$

When the switch is ON we can obtain

$$i_t = i_L$$

And hence, replacing i_L with i_t yields the switch current controller. So for the both of the current

controller(switch and inductor) in the trailing edge modulation we found that :

$$v_1 = v_m \; ; \; v_2 = v_m \; ; \; v_3 = R_s\, i_L \text{ or } R_s\, i_T$$

Table 1. Control value v1, v2, v3 for the general PWM modulator for the various DC-DC converter topologies

Modulation		Converter	Buck-Boost	Boost	Cuk;sepic;zeta
		M(d)	d/(1-d)	1/(1-d)	d/(1-d)
Trailing	i_L ctrl	v_1	v_m	$v_m-R_s\, i_L$	v_m
Trailing	i_T ctrl	v_2	v_m	v_m	$v_m+R_s\, i_L$
Trailing	$<i_T>$ctrl	v_3	$R_s\, i_L$	0	0
Trailing	i_L ctrl	v_1	v_m	$v_m-R_s\, i_T$	v_m
Trailing	i_T ctrl	v_2	v_m	v_m	v_m
Trailing	$<i_T>$ctrl	v_3	$R_s\, i_T$	0	$R_s\, i_T$
Trailing	i_L ctrl	v_1	v_m	$R_s<i_T>$	v_m
Trailing	i_T ctrl	v_2	$v_m+R_s<i_T>$	v_m	$v_m+R_s<i_T>$
Trailing	$<i_T>$ctrl	v_3	0	$-v_m$	0
Leading	i_L ctrl	v_1	$R_s\, i_L$	$R_s\, i_L$	$R_s\, i_L$
Leading	i_D ctrl	v_2	$v_m+2R_s\, i_L$	v_m	$v_m+R_s\, i_L$
Leading	$<i_D>$ctrl	v_3	$-R_s\, i_L$	0	0
Leading	i_L ctrl	v_1	$R_s\, i_D$	$R_s\, i_D$	$R_s\, i_D$
Leading	i_D ctrl	v_2	$v_m+2R_s\, i_D$	v_m	v_m
Leading	$<i_D>$ctrl	v_3	$-R_s\, i_D$	0	$R_s\, i_D$
Leading	i_L ctrl	v_1	$R_s<i_D>$	$R_s<i_D>$	$R_s<i_D>$
Leading	i_D ctrl	v_2	$2R_s<i_D>$	0	0
Leading	$<i_D>$ctrl	v_3	$v_m-R_s<i_D>$	v_m	$v_m+R_s<i_D>$

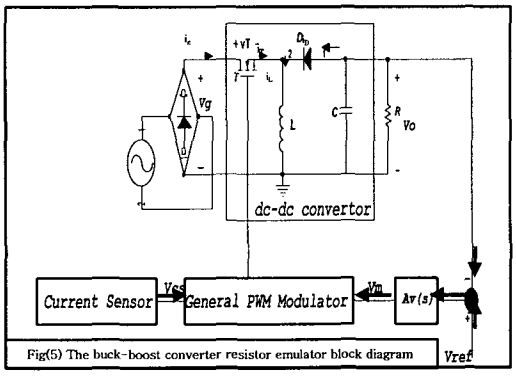

Figure 5. The buck-boost converter resistor emulator block

c) The Cuk converter topology

Figure(6) shows the Cuk converter topology. The control laws of the Cuk converter can be obtain using equ(2) with replacement of M(d)=d/1-d and the input current equal to the input current which yields :

$$v_m = (v_m+R_s<i_L>)d$$

This is the inductor current control. Unlike the other topologies the Cuk converter differs in the switch current as follow :

$$i_t = <i_L>/d$$

the switch current control law is :

$$v_m = v_m d+R_s * i_T * d_2$$

The average switch current control can be derived by replacing

$$<i_t> = d i_T$$

And thus :

$$v_m = (v_m+R_s<i_T>)d$$

For all topologies we can derived the control law for both trailing and leading edge modulations using same procedure. As a result from Table(1) at least one controller for each topology can be implemented with single integrator modulators because

$$v_3 = 0$$

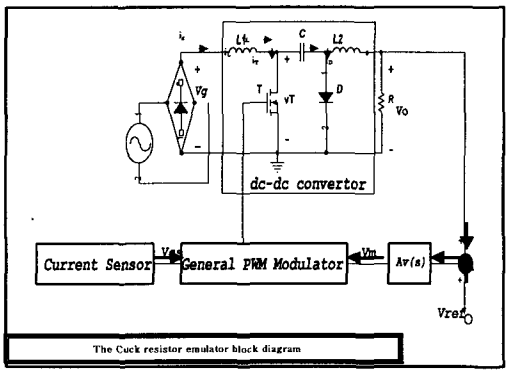

Figure 6. The Cuk resister emulator block diagram

IV. Conclusion

In this paper we cover a family of resister emulator controllers for the quasi steady state. General PWM modulation is presented. Control laws for the quasi steady state are derived. Derivation procedures using both trailing and leading edge modulations are discussed. Five commonly used converters with their control law are listed in Table (1). For these controllers the rectifier line voltage sensor and multiplier that exist in the traditional CCM circuit are eliminated. Therefore, the control circuitry is simplified. The most advantage of these controllers is that their implementation is simplified.

Reference

[1] Z. Lai and K. M. Smedly, "A general constant frequency pulse-width modulator and its application" Sept. 1996.

[2] Robert W. W. Erickson & dragan Maksimovic "Fundamentals of power electronics" jan. 2001.

[3] L. Dixon, "Average current mode control of switching power supplies" Seminar presented at 1990.