Low-Power and Wide-Input Range Voltage Controlled Linear Variable Resistor Using an FG-MOSFET and Its Application

Muneo Kushima, Koichi Tanno, Hiroo Kumagai, Okihiko Ishizuka
Faculty of Engineering, Miyazaki University, Miyazaki, 889-2192, Japan
E-mail: mkushima@esl.miyazaki-u.ac.jp

Abstract: In this paper, a voltage-controlled linear variable resistor (VCLVR) using a floating-gate MOSFET (FG-MOSFET) is proposed. The proposed-circuit is the grounded VCLVR consists of only an ordinary MOSFET and an FG-MOSFET. The advantage of the proposed VCLVR are low-voltage and wide-input range. Next, as applications, a floating-node voltage controlled variable resistor and an operational transconductance amplifier using the proposed VCLVRs are proposed. The performance of the proposed circuits are characterized through HSPICE simulations with a standard 0.6 μm CMOS process. Simulations of the proposed VCLVR demonstrate a resistance value of 40 kΩ to 338 kΩ and a THD of less than 1.1 %.

1. Introduction

Variable resistors are the important circuit elements to compose analog circuits. The grounded variable resistor can be realized by using an MOSFET operated in the linear region. However, the input range of the resistor is very small. In order to improve the problem, several voltage-controlled linear resistors using the MOS technology were proposed[1]–[4].

In the variable resistor proposed by Youssef, the problem was improved [2]. However, this resistor require four supply voltages in order to eliminate non linearities. The problem of the input range was also improved in Moon's variable resistor [3]. The variable resistor is very simple and consists of an ordinary MOSFET and a depletion-mode MOSFET. However, the fabrication cost of the depletion-mode MOSFET is high because the depletion mode MOSFETs cannot be fabricated in the ordinary CMOS process. Recently, Prommee has proposed the new variable resistor based on Moon's variable resistor[3]. However, the power consumption of the variable resistor is higher than that of Moon's one.

In this paper, a new type of voltage-controlled linear variable resistor using an FG-MOSFET is proposed. The proposed resistor is voltage controllable over a high linearity, low power consumption and wide input range. Next, as application of the proposed circuit, a operational transconductance amplifier(OTA) and a floating node VCLVR are presented as applications. The utility of the proposed circuit are evaluated using HSPICE simulations with standard 0.6 μm CMOS process parameters. The simulation results are presented.

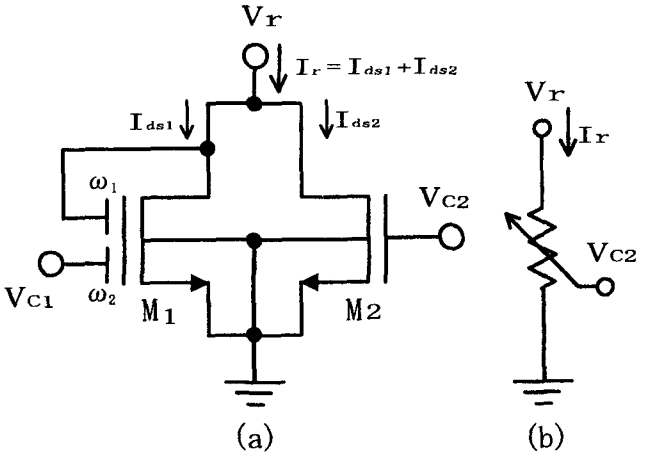

Figure 1. (a)Proposed grounded VCLVR and (b)symbolic representation of the VCLVR.

2. VCLVR

2.1 FG-MOSFET

An FG-MOSFET has important advantages, the multiple-input gates, the variable threshold feature and the fabrication with conventional CMOS process. A threshold voltage seen from one input gate of the transistor is determined by voltages on the other multiple-input gates. When the floating-gate to source voltage (V_{fs}) is larger than the threshold voltage of the FG-MOSFET as seen from the floating-gate (V_T), the drain to source voltage (V_{ds}) is larger than $V_{fs} - V_T$ and the initial charge of the floating-gate equals 0, the FG-MOSFET operates in the saturation region. When the source voltage (V_s) = 0, the drain to source current (I_{ds}) of the k-input FG-MOSFET under the saturation region is given by [5]

$$I_{ds} = \frac{K}{2}\left(\sum_{i=1}^{k}\frac{C_i}{C_0+\sum_{j=1}^{k}C_j}V_i - V_T\right)^2 \quad (1)$$

where K is the transconductance parameter and is proportional to W/L, W is the channel width, L is the channel length, C_i is the capacitance between the floating-gate and i-th input gate, C_o is the oxide capacitance between the floating-gate and the substrate.

2.2 Circuit of Operation

Figure 1 shows the proposed grounded VCLVR. This circuit consists of the 2-input FG-MOSFET and ordi-

nary MOSFET. V_{C1} and V_{C2} shown in Fig. 1(a) are the bias voltages. When M_1 and M_2 operate in the saturation region and the linear region, respectively, drain-to-source current of $M_1(I_{ds1})$ and $M_2(I_{ds2})$ are given by

$$I_{ds1} = \frac{K_1}{2}(\omega_1 V_r + \omega_2 V_{C1} - V_{T1})^2 \quad (2)$$

$$I_{ds2} = K_2\left(V_{C2} - V_{T2} - \frac{V_r}{2}\right)V_r, \quad (3)$$

where K_1 and K_2 are the transconductance parameter of M_1 and M_2, respectively, and V_{T1} and V_{T2} are the V_T of M_1 and M_2, respectively. ω_i is the capacitive weight between the floating-gate and i-th input gate. We assume $V_{T1} = V_{T2} = V_T$. Now, we design K_2 and V_{C1} as like these

$$K_2 = K_1\omega_1^2 \quad (4)$$

$$V_{C1} = \frac{V_T}{\omega_2}. \quad (5)$$

In the last result, the resistance value R of the circuit can be given by

$$R = \frac{1}{K_2(V_{C2} - V_T)}. \quad (6)$$

The theoretical V_r range and the condition of V_{C1} and V_{C2} can be derived by the operation condition of M_1 and M_2, and are given by

$$\begin{aligned} &\omega_1 \leq 1 \\ &V_{C2} \geq V_T \\ &V_{C2} - V_T \geq V_r \geq 0. \end{aligned} \quad (7)$$

On the other hand, it is difficult to realize Eq. (5), because both V_T and ω_2 depends on the fabrication process. We can overcome this problem by using the neuron-MOS V_T cancellation circuit [6]. The cancellation circuit generates the voltage which is just as same as Eq. (5). We can achieve the auto-adjusting scheme by fabricating this circuit into the same chip.

Table 1 Performance of the VCLVR.

Items	Simulation results
Resistance value	40 ~ 338[kΩ] (V_{C2}=1.0 ~ 5.0V)
Power consumption	Same as ordinary resistor 646 μW (V_r=5.0V, V_{C2}=5.0V)
Input range	4.34 V (@V_{C2}=5.0V, THD=1.1%)
	0.34 V (@V_{C2}=1.0V, THD=0.3%)
Bandwidth	2.82 MHz(@V_{C2}=5.0V)
	0.14 MHz(@V_{C2}=1.0V)

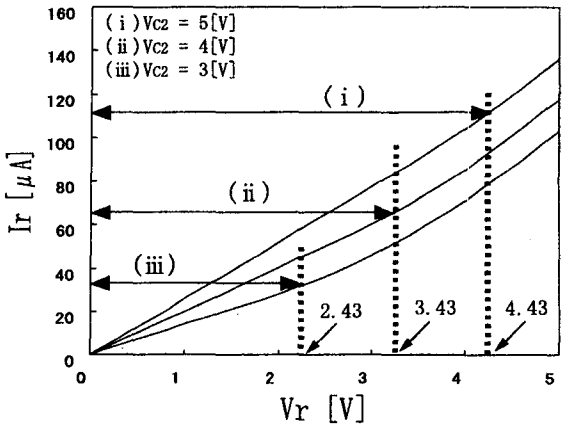

Figure 2. The dc transfer characteristics of the proposed VCLVR (The arrows indicate the theoretical input ranges).

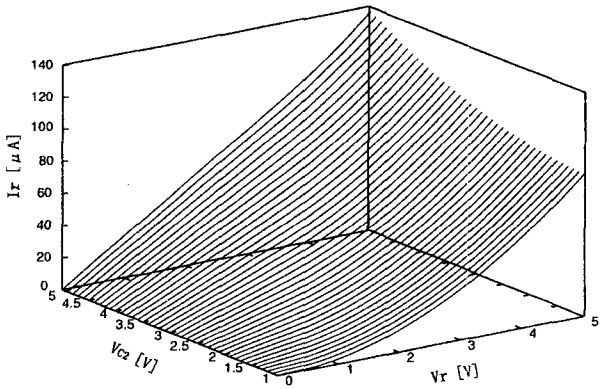

Figure 3. Relationship between I_r, V_{C2} and V_r.

2.3 Simulation Results

In this simulation, W/L of M_1 and M_2 were 20 $\mu m/30$ μm and 3.4 $\mu m/30$ μm, respectively. To satisfy $\omega_1 = \omega_2$, we used a sufficiently large C_1 and C_2, and the value of which was 2.5pF. The bias voltage V_{C1} = 1.4V. The simulated performance of the proposed VCLVR is shown in Table 1. Fig.2 shows the dc transfer characteristics of the proposed VCLVR. The arrows shown in Fig.2 means the theoretical input range derived by Eq.(7). From Fig.2, it is understood that a proposed circuit operates as a voltage-controlled linear variable resistor. Figure 3 shows the relationship between I_r, V_{C2} and V_r under the conditions that V_{C2} and V_r are varied from 1 V to 5 V and 0 V to 5 V, respectively.

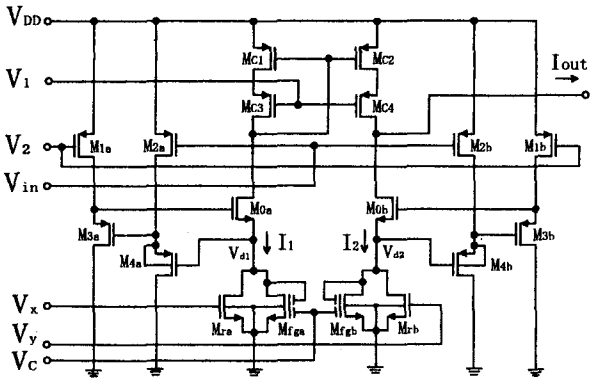

Figure 4. Circuit diagram of the operational transconductance amplifier (OTA) applying the proposed VCLVR, the backgates of all n and p MOSFETs except for $M_{4a,4b}$ are connected to GND and V_{DD}, respectively.

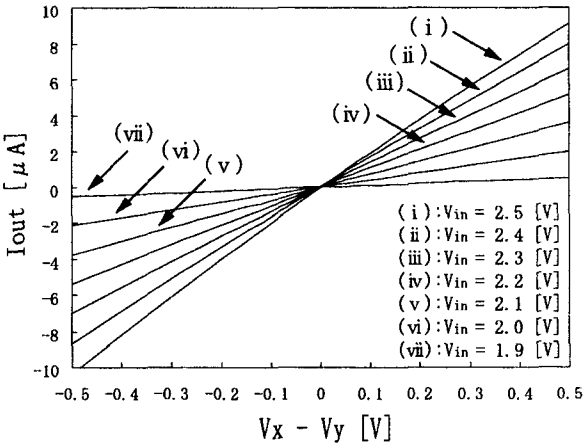

Figure 5. Relationship between I_{out} and V_x - V_y characteristics under the conditions that V_{DD} = 3.0V, V_2 = 1.5V.

3. Applications

3.1 Operational Transconductance Amplifier(OTA)

OTA is a one of the most important circuit element for analog integrated circuits. The good linearity of OTA over wide input range is necessary to extend the application fields of OTA. In this paper, as an application of the proposed VCLVR, OTA is presented. Figure 4 shows the proposed OTA using the proposed VCLVR, including the Crawley's high-swing MOS current mirror. This circuit is based on the regulated cascode circuit with level shift circuit.

When $K_{ia} = K_{ib}$ $(i = 0, 1, \ldots, 4)$, V_{d1} equals V_{d2}. V_d $(=V_{d1}=V_{d2})$ can be given by

$$V_d = V_{in} + V_{DD} + \sqrt{\frac{K_1}{K_3}}(V_{DD} - V_2 + V_{tp}) + V_{tn}, \quad (8)$$

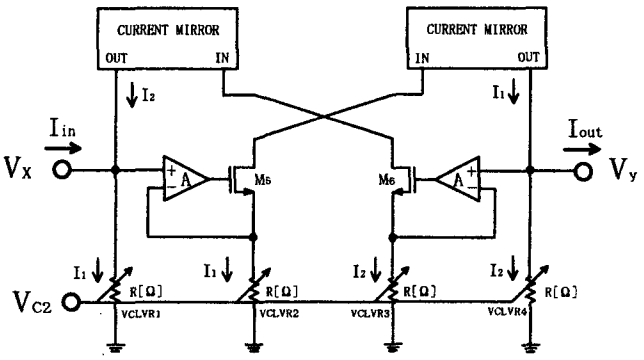

Figure 6. A floating node variable resistor realized by proposed VCLVR.

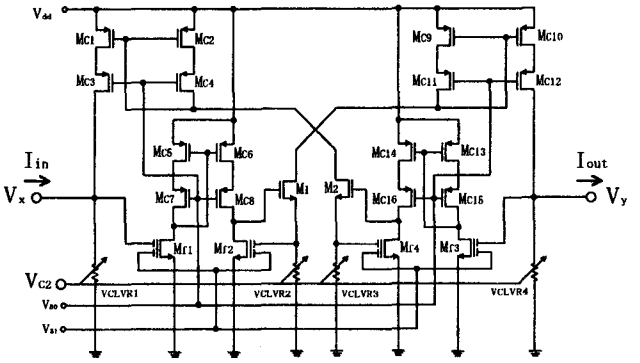

Figure 7. Circuit diagram of the floating node variable resistor applying the proposed VCLVR.

where K_1 and K_3 are transconductance parameter of $M_{1a,b}$ and $M_{3a,b}$, respectively. V_{tn} and V_{tp} are the threshold voltage of n-channel MOSFETs and p-channel MOSFETs, respectively. Consequently, the drain currents of proposed VCLVR are,

$$\begin{aligned} I_1 &= K_2(V_x - V_T)V_d \\ I_2 &= K_2(V_y - V_T)V_d, \end{aligned} \quad (9)$$

where K_2 is K of M_{ra} and M_{rb}. The OTA inputs are their gate terminals V_x and V_y, whereas the OTA output is I_{out} which is difference between I_1 and I_2 in Fig. 4 as follows:

$$\begin{aligned} I_{out} &= I_1 - I_2 \\ &= K_2 V_d (V_x - V_y). \end{aligned} \quad (10)$$

The dc transfer characteristics are shown in Fig. 5 as V_{in} is changed. Simulations of the proposed OTA demonstrate a total harmonic distortion of 1.2%, a -3-dB bandwidth of 30.0 MHz, and a maximum power consumption of 0.22 mW.

3.2 Floating Node VCLVR

Figure 6 shows a floating node variable resistor realized by proposed VCLVR. It has the characteristic that the proposed the floating node variable resistor circuit can operate from zero level voltage. Figure 7 is the

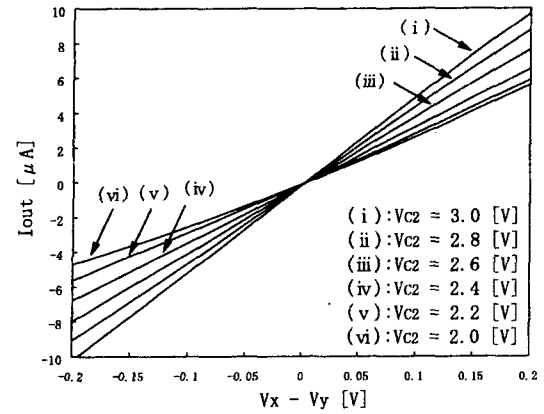

Figure 8. Relationship between output current, I_{out} and terminal voltage, V_x - V_y.

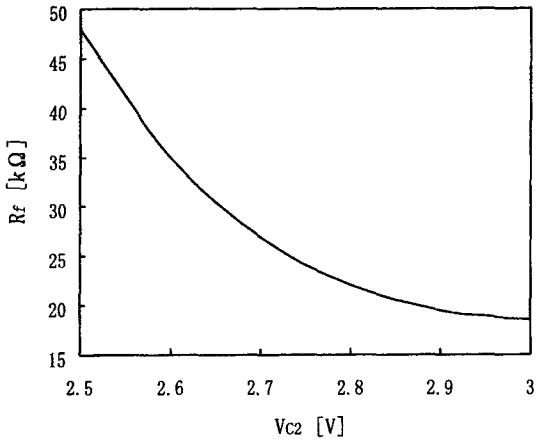

Figure 9. Relationship between bias voltage, V_{C2} and resistance value, R_f.

circuit diagram of the floating node variable resistor applying the proposed VCLVR. In Fig. 7, we assume that the corresponding MOSFETs between the left and right half circuits are perfectly matched and that each MOSFET obeys a square law in the saturation region and the channel length modulation effect of each MOSFET can be ignored. From Fig. 7, Kirchhoff's current law at the V_x and V_y terminals gives

$$\begin{aligned} I_{in} &= I_{out} \\ &= K_2(V_{C2} - V_T)(V_x - V_y). \end{aligned} \tag{11}$$

Therefore, the value of a floating node variable resistor R_f is given by

$$\begin{aligned} R_f &= \frac{V_x - V_y}{I_{in}} \\ &= \frac{1}{K_2(V_{C2} - V_T)}. \end{aligned} \tag{12}$$

As Eq.(12) shows, the value of R_f can be designed by V_{C2}. And this value is the same as Eq.(6). From the above analysis, one can see that a realized resistor is a floating node variable resistor.

Figure 8 shows the dc transfer characteristics for when the V_y - terminal voltage is fixed to 1.0 V. And it shows that the proposed circuit gives resistance and its value tunable by V_{C2} in Fig. 8. Figure 9 shows the relationship between V_{C2} and R_f. The resistance values of 18.5 kΩ to 48.0 kΩ can be obtained with 2.5 V $\leq V_{C2} \leq$ 3.0 V from Fig. 9.

4. Conclusion

In this paper, we have proposed a simple circuit configuration to realize a low-power and wide-input range voltage controlled linear variable resistor using an FG-MOSFET. Also, an OTA and a floating node VCLVR are proposed as applications. The performance of the proposed-circuits are characterized through HSPICE simulations with a standard 0.6 μm CMOS process.

The fabrication and measurement of the proposed circuits are topics for further study.

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