Anti-fuse program circuits for configuration of the programmable logic device

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Abstract: In this paper, we designed the anti-fuse program circuit, and there are an anti-fuse program/sense/ latch circuit, a negative voltage generator, power-up circuit and etc. in this circuit. An output voltage of a negative voltage generator is about −4.51V. We detected certainly it regardless of simulation result power rise time or temperature change to detect the anti-fuse program state of an anti-fuse program/sense/latch circuit and were able to know what performed a steady action. And as a result of having done a simulation while will change a resistance value voluntarily in order to check an anti-fuse resistance characteristic of this circuit oneself, it recognized as a programmed anti-fuse until 23kΩ, and we were able to know that this circuit was a lot of margin than general anti-fuse resistance 500Ω. Therefore, the anti-fuse program circuit of this study showed that was able to apply for configuration of the programmable logic device.

1. Introduction

Recently, the information & communications has been high-speed and mass. The method of information & communication are the PCS, the personal computer communication and the optical communication. Also, HDTV is sending information using TV broadcast. Communication industries of the world are forecasting an explosive transmission speed and an increase of an amount of information according to development of the Internet, the multimedia and the mass media[1].

The use of various logic circuit and memory device is unavoidable in an information communication system. Various logic circuits and memory chips can be selectively used in configuration of an information communication system. Particularly, the selective use of the logic circuits and the configuration elements are unavoidable while a system becomes the SOC(System On Chip) recently. Therefore, the program circuit in order to be selectively usable is required particularly, and the element, which was fuse or anti-fuse, is used in this program circuit[2-3].

Anti-fuse is the element that became conductor/insulator/ conductor structure. It operates only with capacitor before rupture of an insulator in this structure, and was open state(off state) electrically. The short state(on state) that both conductors are connected after rupture of an insulator. Anti-fuse is the memory element such as PROM (programmable read only memory) showing a semipermanent open state or short state, is the program switch element which selectively connect logic blocks in FPGA(Field Programmable Gate Array). Also, it is used as an function element to relieve defect memory cell to occur from a process of DRAM(Dynamic Random Access Memory)[3-5].

We call a rupture action of the anti-fuse insulator programming. Programming is performed electrically and lets this approves the high voltage between the both end conductors that are not a cutting of the fuse using laser, and rupture happen. A rupture voltage, a programming voltage, is announced with 7~20V according to a process technology and insulating materials producing anti-fuse[4-5]. Figure 1 shows the method of program using high voltage and a laser.

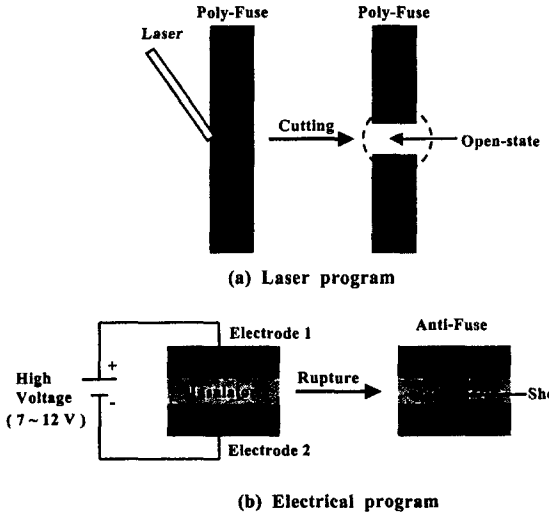


Figure 1. Program method of fuse (a) a laser program (b) an electrical program

We designed the antifuse-program circuit[6-7] in this study and we present an action way of this circuits and measure action characteristic through a simulation. Also, the circuit which designed is going to present that it is possible to applicate for configuration of the programmable logic device.

2. Circuit Design

In this paper, insulating materials of used anti-fuse are ONO(Oxide/Nitride/Oxide), and it is PIP(Poly/Insulator/ Poly) structure. The resistance of this anti-fuse has several

GΩ or above at the time of regular state, and has 500Ω or below after program. In case of this, a program voltage of anti-fuse is 6.7~7.2V, and a program is performed within one second[6]. Therefore, an anti-fuse program circuit is designed according to this condition.

Figure 2 shows block diagram of an electrical program circuit. A total block divides into it to three parts in the action side. A first part is a circuit to program anti-fuses, and this is composed of an address decoder, a negative voltage generator and the oscillator that generate periodic clock pulse and supply to a voltage generator. The second part is a control circuit to need in order detect the program or not of anti-fuse, and there are a power rise sense circuit(PUD : Power Up Detector) generating a signal to need in order to detect the state of anti-fuse for stabilization duration of a power voltage. The last part has an anti-fuse program/sense/latch(APSL) circuit.

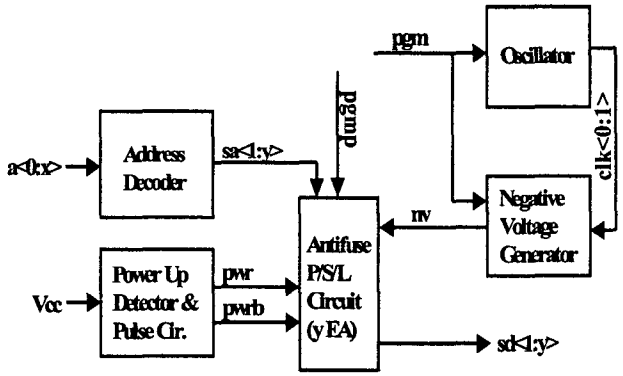
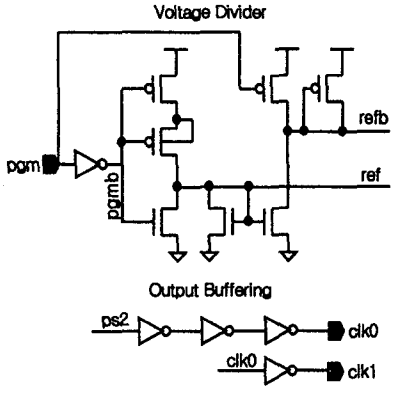


Figure 2. Block diagram of an anti-fuse program circuit

Figure 3 is oscillator this which generates clock pulse necessary for voltage generator. This oscillator is controlled a pulse generation section with a voltage as having remodeled general ring oscillator, and please increase he pulse cycle. This oscillator can reduce number of inverter generating pulse and can reduce a consumption area. Figure 4 is a negative voltage generator which generates negative voltage for program anti-fuse. If anti-fuse program signal *pgm* becomes 'high', a negative voltage generator starts an action, and an output signal of oscillator is input at the time of this.



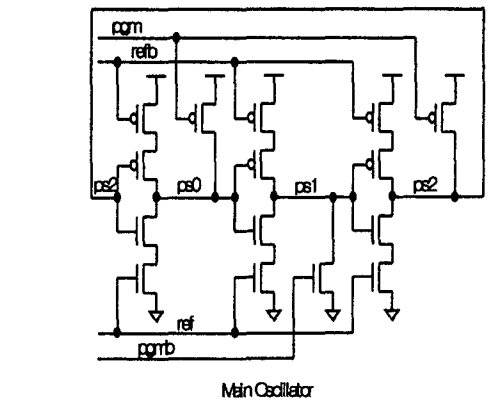


Figure 3. Oscillator

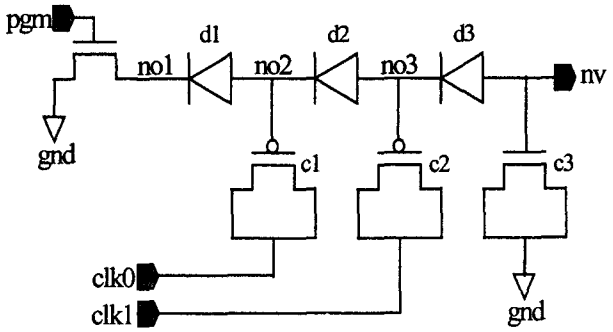


Figure 4. A negative voltage generator

If an anti-fuse program action is over, an anti-fuse program circuit gets power off done and performs power on again. A power rise time is different, and every each system has time of several hundred ms in number ns. The power rise search circuit that generate a 'high' signal if power(Vcc) become an established voltage(2Vt, threshold voltage) or above. It is detected the program or not of anti-fuse by two pulse signal *pwr* and *pwrb*, and the signals have each other an objection phase. And detected data is latched. Figure 5 is power rise search and pulse circuit.

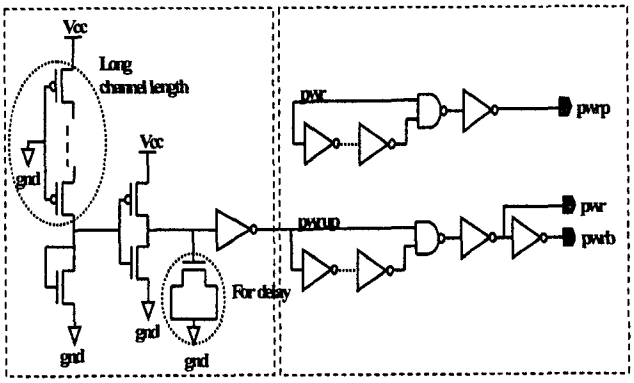


Figure 5. Power up detector and pulse circuit

It is the anti-fuse program/sense/latch circuit that used an output voltage of a negative voltage generator shown figure 6. This circuit is using a electric potential difference of power voltage(Vcc) and output voltage(*nv*) of a negative voltage generator so that program does anti-fuse. The

voltage adjustment signals of this circuit are *pgmp* input to be happened with 'high' pulse of number ns when program start singal (*pgm*) becomes 'high' and 'high' signal of *sa*(special address) to select only one during multiple anti-fuses. At the same time, *pwr* is 'low', and *pwrb* is 'high'. If a *pgm* signal becomes 'high', a negative voltage generator runs action and *pgmp* sends 'high' pulse signal at the same time and makes a voltage of node *ao1* from 0V. If output *nv* of a voltage generator drops below –4V and sends a *sa* address to select anti-fuse from a SAD circuit, the Vcc voltage is supplied to anti-fuse one electrode, and the *nv* voltage is supplied to other electrode, and then program starts.

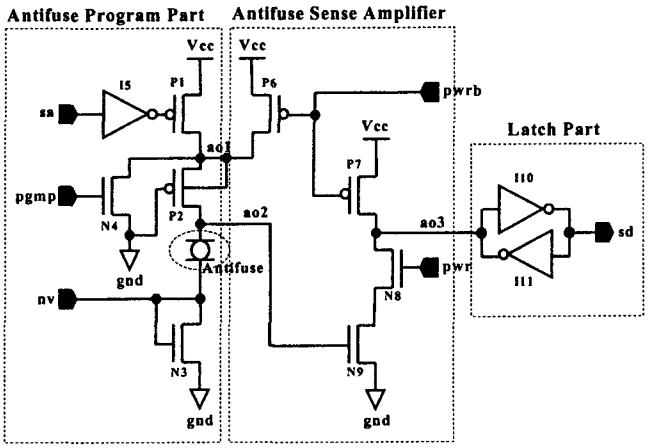


Figure 6. Anti-fuse program/sense/latch circuit

If anti-fuse program action is over all, off gets power done and performs power on again. If *pwrup* becomes 'high' during power stabilization duration, *pwr* displays 'high' pulse and *pwrb* displays 'low' pulse, and it is supplied the Vcc voltage to anti-fuse (node *ao2*). If an anti-fuse became program, the node *ao2* voltage is connected with grounding(gnd) path, and it is had 'low' voltage, but if an anti-fuse did not became program, the node *ao2* voltage had 'high' voltage. Therefore, if an anti-fuse became program, though *pwr* is 'high', but because node *ao2* has low voltage, node *ao3* becomes 'high', and output *sd* becomes 'low'. And if an anti-fuse did not become program, as for the *sd*, it is displayed 'high'.

3. Result and Consideration

As for the period of clock pulse that was based on a temperature as a result that we use HSPICE tool and a simulation did the designed oscillator of voltage control type, is 27±5ns and therefore is same as a table 1. If a temperature rises, a clock period slow, it is because *ref* and *refb* node potential difference grow larger. Also, a clock period changes according to the Vcc change, and we can know that a clock period is fast because a action speed of MOS is fast according to Vcc rising because a action principle of MOS is a voltage control way.

The output *nv* appeared with −4.51V as a result that a simulation did a negative voltage generator in condition of 25°C and 3.3V(Vcc). Therefore, we can know that it satisfy program voltage 7.5V if it uses their potential difference, because Vcc voltage is with 3.3V and *nv* voltage is with −4.51V when program does anti-fuse.

Table 1. Clock pulse period

	Temp. [°C]			Vcc [V]		
	−10	25	90	2.5	3.3	4.0
refb [V]	2.09	2.15	2.25	1.47	2.15	2.75
ref [V]	1.03	0.99	0.96	1.03	0.99	1.09
Clock period [ns]	23	27	33	31	27	23

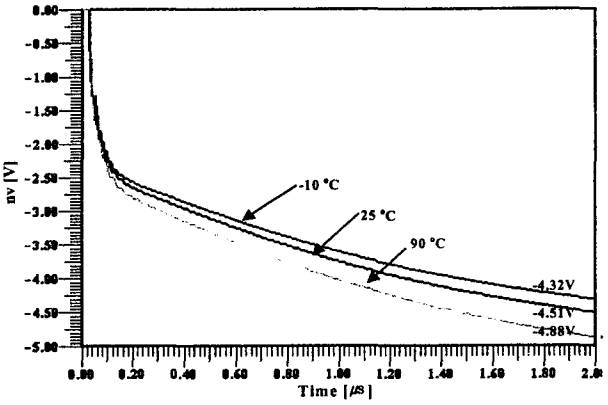


Figure 7. Simulation results of a negative voltage generator

We assumed that resistance of a programmed anti-fuse is 1kΩ and capacitance of a unprogrammed anti-fuse is 50fF in order to simulation an anti-fuse program/sense/latch circuit of a negative voltage way . In the simulation result of a power-up pulse circuit, each pulse width appeared with 30.38ns and 31.25ns in condition of 3.3V(Vcc) and 25°C, and if power-up time is done slow by 200ms, it is increased by 1us. This cause is because a delay width of power-up pulse circuit is increased because an initial high voltage of a *pwrup* signal displayed in a power-up detection circuit is very 'low' with 1.2V.

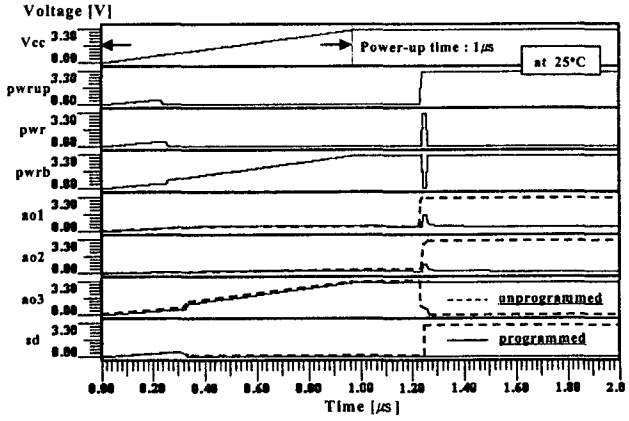


Figure 8. Simulation results of an APSL circuit

Table 2 is the simulation result according to a temperature in condition that sets up Vcc as 3.3V and power-up time as 10us in order to measure to recognize as a programmed

anti-fuse when an anti-fuse resistance have how much in an anti-fuse program/sense/latch circuit. And a resistance of anti-fuse is recognizing that program became until 23~38kΩ according to a temperature.

Table 2. Resistance simulation results of an APSL circuit

Temp.	-10°C	25°C	90°C
Programmed	23 kΩ	28 kΩ	38 kΩ
Unprogrammed	24 kΩ	29 kΩ	39 kΩ

Therefore, it recognize a programmed one if a resistance of anti-fuse becomes 23kΩ or below in this circuit. We can know what the designed circuit is securing a lot of margin about an anti-fuse resistance because the resistance appeared with 500Ω or below when the made anti-fuse did program with 7.5V.

4. Conclusion

We designed the program circuit which introduced anti-fuse for the logic device configuration that program was possible and designed in order to be able to do enough program even if a circuit proposed to used a lot of anti-fuse elements. As a result of having measured an action characteristic of designed circuits, we got the following conclusion. Through the conclusions we was able to know that an anti-fuse program circuit designed was suitable for configuration of the programmable logic device.

1. The clock pulse period of oscillator appeared with 27ns, and an output voltage of a negative voltage generator was about -4.51V, and we was able to know that it was usable with an enough program voltage because a electric potential difference between anti-fuse both ends became 7.5V or over if it used a power voltage as 3.3V.
2. We was able to know that performed a steady circuit action because it certainly detected the programmed anti-fuse or not in simulation result regardless of power rise time and temperature change of an anti-fuse program/sense/latch circuit.
3. Anti-fuse program circuits are very stable and are applicable to any process technology like to DRAM, FPGA, and etc.

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