A 900㎒ RF CMOS Power Amplifier for Wireless One-chip Tranceiver

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Abstract : Power amplifier of wireless communication tranceiver can be effectually controlled output power. And small size and low power dissipation are indispensable to portable system. In this paper, to reduce the size of portable tranceiver, inductor is integrated in a single chip. And to reduce power dissipation, a power amplifier that can be digitally controlled output power, is proposed and designed.

1. Introduction

In these days, popularity of wireless communication tranceiver for portability has been increased . The main research area of it is realization of small size, low voltage, low power and low price. So main solution of all problem is integration of all communication blocks at one single chip[1]-[5]. In this paper, power amplifier of RF communication system blocks is proposed and designed by using CMOS process . Generally, power amplifier characteristics using CMOS process is not adequate for RF systems. So, it is made with GaAs of compound semiconductor. But it has many weak pints of high price and high voltage operation.

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Also, because major block of RF system is made with CMOS process, single chip integration with GaAs process is almost impossible. So making power amplifier by CMOS process is getting more and more important part and it will play main role to realize the small size, low price and low voltage of wireless communication tranceiver.

2. Design of Power Amplifier

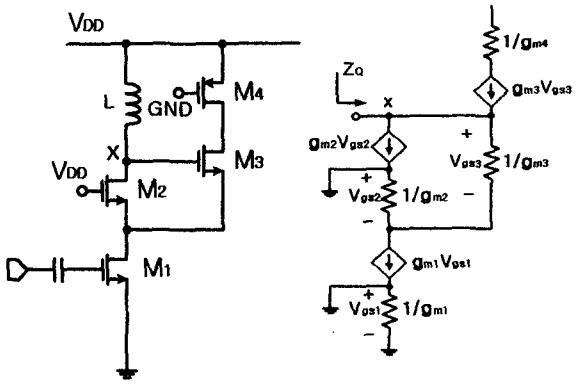
Proposed power amplifier in this paper is designed with pre-amplifier and spiral inductor.

2.1 Pre-Amplifier

Q-enhancement circuit of proposed power amp. is used to get the high voltage gain at input stage. Also, it reduces power dissipation & Miller effect at input stage. So that high operation frequency is acquired . Figure 1 is proposed Q-enhancement circuit in this paper.

$$Z_Q = -\frac{g_{m2} + g_{m3}}{g_{m2}\, g_{m3}} \qquad (1)$$

$$G_{tot} = \frac{R_s}{(\omega L)^2} + Y_Q = \frac{R_s}{(\omega L)^2} - \frac{g_{m2} g_{m3}}{g_{m2} + g_{m3}} \qquad (2)$$



(a) Q-enhancement circuit

(b) Small-signal model at Q-enhancement circuit

Fig. 1. Proposed Q-enhancement circuit

High gain can be obtained at node X by peaking generation due to LC resonance of parasitic capacitance and inductor. But because low Q of inductor increases the loss of gain, Q-enhancement circuit in figure 1 compensates for gain loss by series resistance of metal. The value of Q of spiral inductor is mainly effected by loss due to substrate and series resistance of metal.

Figure 1 is Q-enhancement circuit and its small-signal model. Equation (1) is impedance Z_Q at node X. Equation (2) is total conductance including series resistance of inductor.

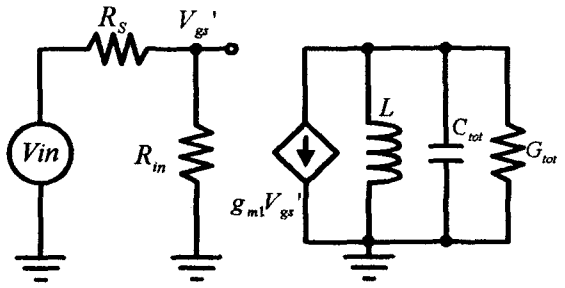


Fig. 2. Small-signal model of Q-enhancement circuit

$$A_v = -\frac{R_{in}}{R_s + R_{in}} \frac{g_{m1}}{G_{tot}} \quad (3)$$

Figure 2 is small signal model of Q-enhancement circuit. Equation (3) is derived from small signal model of Fig. 2. In Fig.2 , if series resistance of inductor and all parasitic component are coincided with negative conductance of Q-enhancement circuit, then the gain will become infinite.

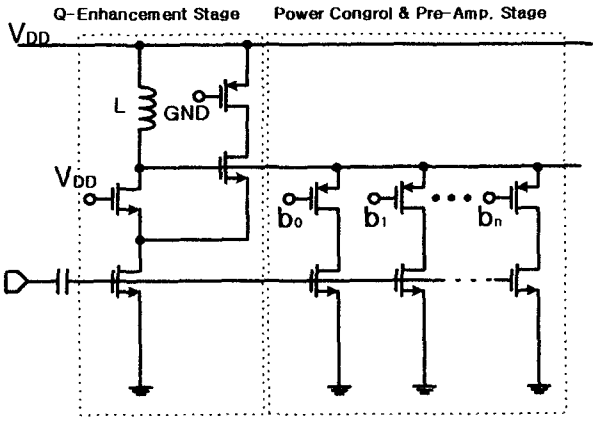


Fig. 3. Switch mode pre-amplifier stage for controlling output power

Figure 3 is proposed switch mode multi pre-amplifier circuit for digitally controlling output power in this paper. Conventionally, to control the output power, bias voltage adjustment of output-stage transistor, magnitude control of gate input signal and digitally programming method for required power, are used[1]. But the method of selective controlling the output power is used in this paper by using various amplifier stage which have different gain each other.

2.2 Inductor

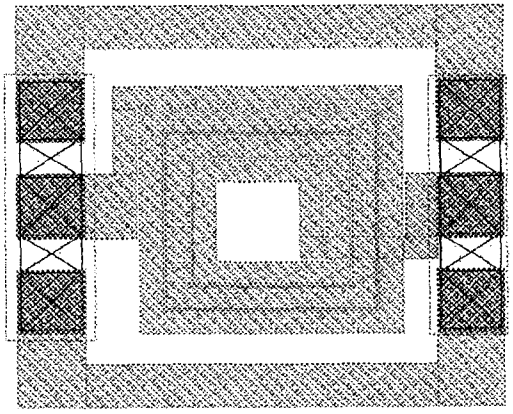


Fig. 4. Layout of inductor

Optimal performance of spiral inductor is designed with computer simunation for optimized turns number, space of metal, inside diameter, outside diameter and width of metal lines(width). Designed spiral inductor using ASTIC simulation is shown in Fig. 4 .

3. Simulations Results

To get the correct HSPICE simulation, parasitic capacitance of pad and pi-equivalence model of spiral inductor are added. From the results of simulation, we know that output power is increased from 3 dBm to 13.5 dBm for all switch of input stage ON.

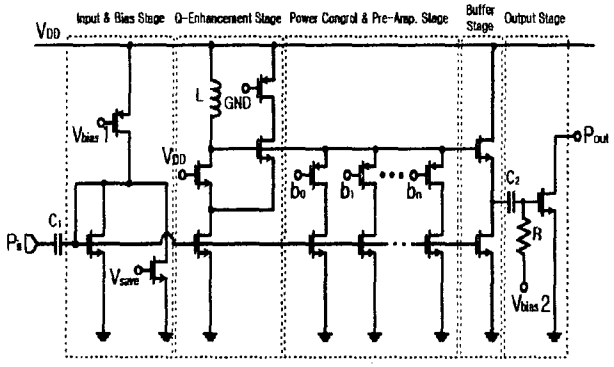


Fig. 5. Circuit of designed power amplifier

Figure 5 is proposed circuit of power amplifier. And figure 6 shows the output power depending on input frequency. Magnitude of output power can be controlled in digital mode.

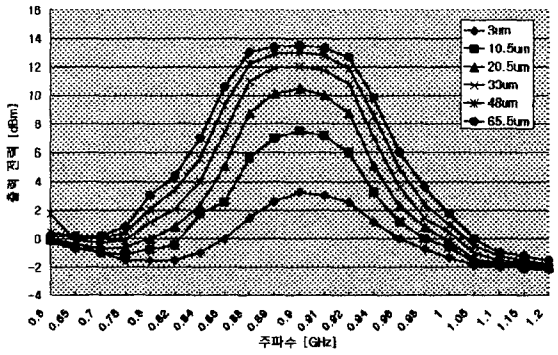


Fig. 6. Output power of designed power amplifier depending on input frequency

Figure 7 shows the simulation results of output power control characteristics at 3 voltage source. From the results, we know that power control range of 10 dBm is acquired.

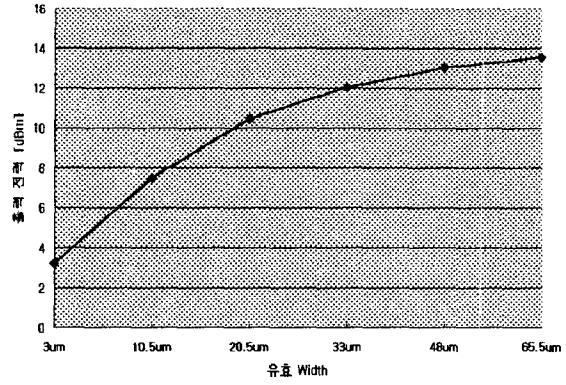


Fig. 7. output power control range

Figure 8 shows the PAE(Power Added Efficiency) characteristic depending on output power at 3V and 900㎒ input. From the results of simulation, designed power amplifier has 55% PAE at maximum output power of 13.5 dBm.

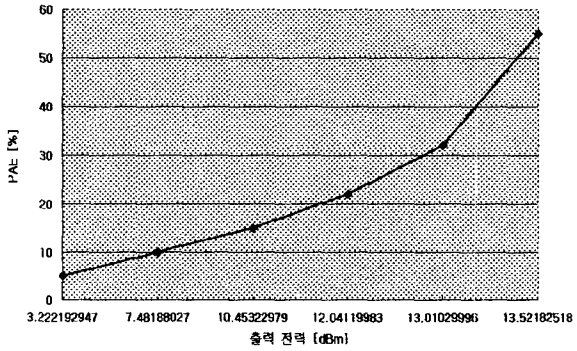


Fig. 8. PAE characteristic by output power

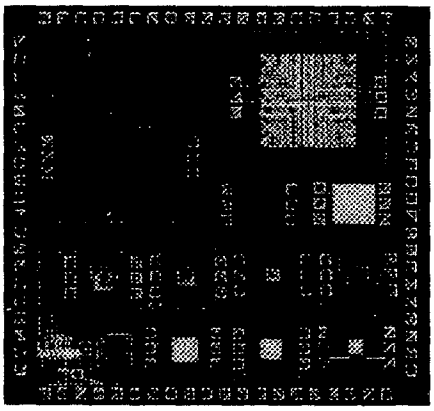


Fig 9. Layout of designed power amplifier

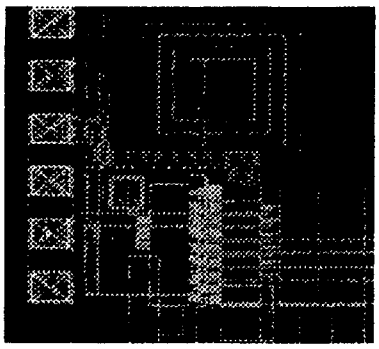


Fig. 10 The part of designed power amplifier

4. Conclusions

Power amplifier for wireless one-chip tranceiver is proposed and designed by using 0.6㎛ CMOS process. Figure 9 is all layout considering the testing. The designed power amplifier utilize the integrated spiral inductor as load and can be controlled output power digitally. Also, it has pre-amplifiers with low voltage bias and class-C output stage.

From the results of simulation, maximum power is increased from 3.5dBm to 13.5dBm(3V power supply voltage, 900㎒ input frequency) and it has maximum 13.5dBm PAE when all input stage of pre-amplifier is on. Proposed and designed power amplifier in this paper is now processing by 0.6㎛ CMOS process.

Reference

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