Design of Subband Image Encoder by Discrete Wavelet Transform

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Abstract

Introduction of digital communication network such as Integrated Services Digital Networks(ISDN) and digital storage media have rapidly developed. Due to a large amount of image data, compression is the key techniques in still image and video using digital signal processing for transmitting and storing. Digital image compression provides solutions for various image applications that represent digital image requiring a large amount of data. In this paper, the proposed DWT(Discrete Wavelet Transform) filter bank is consisted of simple architecture, but it is efficiently designed that a user obtains a wanted compression rate as only input parameter. If it is implemented by FPGA chip, the designed encoder operates in 12MHz.

I. INTRODUCTION

All methods for Compression is based on two fundamental principles. One principle is to use the properties of signal source and to remove redundancy from the signal. When considering digital images as realizations of two-dimensional stochastic process, this structure manifests itself through statistical dependencies between pixels. The other principle is irrelevancy reduction that is to exploit the properties called human visual system that is not perfect and to omit parts or details of the signal that will not be noticed by the receiver[3] [7].

The theory of subband decomposition provides an efficient framework for the implementation of schemes for redundancy and irrelevancy reduction. It has been demonstrated repeatedly in subband and wavelet based schemes. Nevertheless, most of today's image and video coding standards use the Discrete Cosine Transform (DCT) for signal decomposition. However, it is not sufficient for next generation image compression and transmission. The important motives of using subband decomposition schemes are the demand for a "scalable" image representation [4].

The subband image decomposition using wavelet transform has a lot of advantages. Generally, it profits analysis for non-stationary image signal and has high compression rate. And its transform field is represented multiresolution like human's visual system so that can progressively transmit data in low transmission rate line.

In this paper, it is implemented by FPGA using Altera chip, after VHDL coding of DWT encoder for image processing. It uses filter bank pyramid algorithm for wavelet transform and can speed up as each filter consists of the FIR filter and two filters are connected with parallel structure that can compute lowpass and highpass DWT coefficients in the same clock cycle. Because of using QMF properties, it reduces half number of the multiplier needed DWT computation. It can increase efficiency as well as reduce hardware size. Also, because memory controller required in multisolution decomposition is designed by hardware, a user can manipulate the designed encoder only input parameter.

II. REVIEW OF DWT

The wavelet transform is a new mathematical tool developed mainly since the middle of the 1980s. The wavelet transform provides multiresolution analysis with dilated windows. The high frequency analysis is done using narrow windows and the low frequency analysis is done using wide windows.

The wavelet function is generated by translating and dilating basis functions called mother wavelet. The wavelet basis is generated from the scaling function basis. If it suffices admissible condition, it forms orthonormal basis in $L^2(R)$. The orthonormal basis is a set of basis elements that generate any element of the set, do not concern among elements and element norm of the basis is one [2].

The DWT is computed by convolution and decimation series recursively. When computing DWT of discrete time data, input data is DWT coefficients from the high resolution stage. Eq.1 is used to compute DWT coefficients of subsequent stage. In practice, this

decomposition is performed only for a few stages. We note that the dilation coefficients H(z) represent a lowpass filter(LPF), whereas the corresponding G(z) represent a highpass filter(HPF). Input sequences, $C_{j-1}(n)$ in each scale level j feed in highpass filter and lowpass filter respectively. $D_j(n)$, the output from highpass filter represent the details of input sequences. $C_j(n)$, the Output from low pass filter represent the averages of input sequences. In Eq.4, G(z) and H(z) is Z-transform that is represented by scaling function and wavelet function which are represented by a set of coefficients. Eq.1 is the sequential DWT algorithm[2] .

$$C_j(n) = \sum_n H(n-2k)C_{j-1}(n)$$
$$D_j(n) = \sum_n G(n-2k)C_{j-1}(n) \quad (1)$$

$$G(n) = (-1)^n H(N-n) \quad (2)$$

As shown in Eq.2, the wavelet filter coefficients is obtained from alternating flip of scaling filter coefficients[2]. To reconstruct original data, the DWT coefficients are upsampled and go through another set of lowpass and highpass filter(Eq.3).

$$C(n,j) = \sum_n C(k,j+1)H'(n-2k) + \sum_l D(l,j+1)G'(n-2l) \quad (3)$$

$$H(z) = h_0 + h_1 z^{-1} + h_2 z^{-2} + h_3 z^{-3}$$
$$G(z) = g_0 + g_1 z^{-1} + g_2 z^{-2} + g_3 z^{-3} \quad (4)$$

In this paper, the Daubechies wavelet algorithm is used for computing DWT coefficients. FIR filter transfer function of Daubechies 4 is expressed to Eq.4 and filter coefficients is shown in table 1.

Table 1. Filter Coefficients of Daubechies wavelet

N	H	G
0	0.48296291314453	0.12940952255126
1	0.83651630373781	0.22414386804201
2	0.22414386804201	-0.83651630373781
3	-0.12940952255126	0.48296291314453

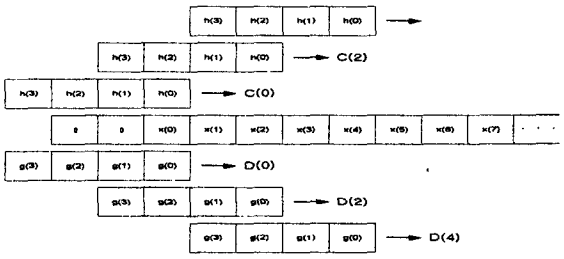

Fig.1. Data flow block diagram

As shown in Eq.1, the DWT computation is rather complex because of the data dependencies at different stage. Fig.1 is shown data flow block diagram of DWT computation in the DWT filter.

As shown in Fig.1, output data from the first stage to the third stage can be expressed as follows :

The first stage

$$\begin{aligned}
G_0(0) &= g(0)a(0) + g(1)a(-1) + g(2)a(-2) + g(3)a(-3)\\
G_0(2) &= g(0)a(2) + g(1)a(1) + g(2)a(0) + g(3)a(-1)\\
G_0(4) &= g(0)a(4) + g(1)a(3) + g(2)a(2) + g(3)a(1)\\
G_0(6) &= g(0)a(6) + g(1)a(5) + g(2)a(4) + g(3)a(3)\\
G_0(8) &= g(0)a(8) + g(1)a(7) + g(2)a(6) + g(3)a(5)\\
G_0(10) &= g(0)a(10) + g(1)a(9) + g(2)a(8) + g(3)a(7)\\
G_0(12) &= g(0)a(12) + g(1)a(11) + g(2)a(10) + g(3)a(9)\\
H_0(0) &= h(0)a(0) + h(1)a(-1) + h(2)a(-2) + h(3)a(-3)\\
H_0(2) &= h(0)a(2) + h(1)a(1) + h(2)a(0) + h(3)a(-1)\\
H_0(4) &= h(0)a(4) + h(1)a(3) + h(2)a(2) + h(3)a(1)\\
H_0(6) &= h(0)a(6) + h(1)a(5) + h(2)a(4) + h(3)a(3)\\
H_0(8) &= h(0)a(8) + h(1)a(7) + h(2)a(6) + h(3)a(5)\\
H_0(10) &= h(0)a(10) + h(1)a(9) + h(2)a(8) + h(3)a(7)\\
H_0(12) &= h(0)a(12) + h(1)a(11) + h(2)a(10) + h(3)a(8)
\end{aligned} \quad (5)$$

The second stage

$$\begin{aligned}
G_1(0) &= g(0)G_0(0) + g(1)G_0(-2) + g(2)G_0(-4) + g(3)G_0(-6)\\
G_1(2) &= g(0)G_0(4) + g(1)G_0(2) + g(2)G_0(0) + g(3)G_0(-2)\\
G_1(4) &= g(0)G_0(8) + g(1)G_0(6) + g(2)G_0(4) + g(3)G_0(2)\\
G_1(6) &= g(0)G_0(12) + g(1)G_0(10) + g(2)G_0(8) + g(3)G_0(6)\\
H_1(0) &= h(0)H_0(0) + h(1)H_0(-2) + h(2)H_0(-4) + h(3)H_0(-6)\\
H_1(2) &= h(0)H_0(4) + h(1)H_0(2) + h(2)H_0(0) + h(3)H_0(-2)\\
H_1(4) &= h(0)H_0(8) + h(1)H_0(6) + h(2)H_0(4) + h(3)H_0(2)\\
H_1(6) &= h(0)H_0(12) + h(1)H_0(10) + h(2)H_0(8) + h(3)H_0(6)
\end{aligned} \quad (6)$$

The third stage

$$\begin{aligned}
G_2(0) &= g(0)G_1(0) + g(1)G_1(-2) + g(2)G_1(-4) + g(3)G_1(-6)\\
G_2(2) &= g(0)G_1(4) + g(1)G_1(2) + g(2)G_1(0) + g(3)G_1(-2)\\
G_2(4) &= g(0)G_1(8) + g(1)G_1(6) + g(2)G_1(4) + g(3)G_1(0)\\
H_2(0) &= h(0)H_1(0) + h(1)H_1(-2) + h(2)H_1(-4) + h(3)H_1(-6)\\
H_2(2) &= h(0)H_1(4) + h(1)H_1(2) + h(2)H_1(0) + h(3)H_1(-2)\\
H_2(4) &= h(0)H_1(8) + h(1)H_1(6) + h(2)H_1(4) + h(3)H_1(2)
\end{aligned} \quad (7)$$

III. HARDWARE ARCHITECTURE

The proposed DWT encoder in this paper processes input 8bit data that is original image. Greatly, it consists of two blocks. One is the DWT filter bank that consist of normalization block which convert image data to floating point and select input image and RAM data, hardwired coefficient register, filter bank which computes DWT coefficients of highpass and lowpass and downsampler. The other is the memory controller that consists of the separated read and write address counter for RAM READ/WRITE operation, the controller which receives parameter value and controls system and data/address selector which selects READ/WRITE address of the separated RAM.

i. DWT FILTER BANK

The process for the highpass and lowpass DWT coefficient

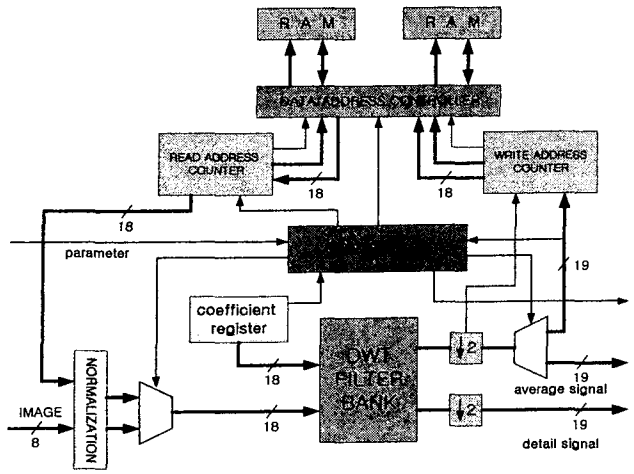

Fig. 2. System block diagram

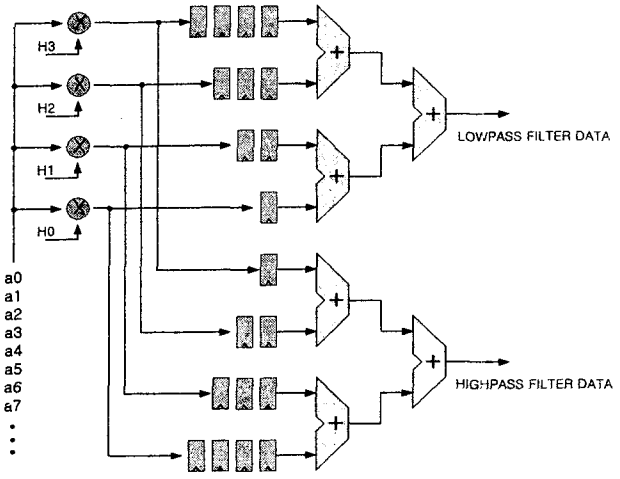

Fig. 3. DWT filter bank

computation can obtain from filter bank that consists of simple FIR filter with adder and multiplier(Fig.2). As shown in Eq.2, because highpass and lowpass filter coefficients satisfy PR(Perfect Reconstruction) conditions with QMF properties, the highpass filter coefficients obtain from lowpass filter coefficients. This characteristics is efficiently used the proposed architecture in this paper.

In the point of hardware, because the speed of the system clock depends on a multiplier, the design of multiplier is very important. The multiplier in the proposed encoder uses the modified radix-4 booth algorithm. The adder and multiplier used the FIR filter makes use of 18 bit floating point that consists of mantissa 11 bit, exponent 6 bit and sign 1 bit.

As shown in Fig.2, the proposed encoder has an efficient structure that is implemented by one filter cell for multiresolution. Fig.3 represents DWT filter block diagram. The input data feeds in the multiplier that has parallel structure for high speed processing without delay. After converting sign bit (Eq.2), the output data through the multiplier feeds in a part of delay using floating point advantages for highpass and lowpass DWT coefficients computation. The signal through out lowpass filter is an important bit more than point to reconstruct original signal because it is $\sqrt{2}$ times. The signal through out highpass filter low is an important bit less than point to reconstruct original signal because it approaches near zero. If the proposed encoder is designed by fixed point, it requires additional control circuit to identify the point location. A floating point expression of number can extend expressible range. And each filter composed different coefficients of filter bank can multiply without special care. Therefore, users can control it easily and obtain the multiplied result with high precision.

As shown in the Fig.3, The proposed DWT filter bank can reduce by half the number of multiplier used for computing highpass and lowpass DWT coefficients. This is the result that it is not located in the front but the back. It is the result using QMF characteristics and can obtain the same speed when comparing a parallel structure with the proposed DWT filter bank. If the applications such as video processing using the DWT use the systolic array implemented one filter, it needs twice as slow as the system clock cycle for highpass and lowpass DWT coefficient computation. This is not efficient in the point of hardware size to clock speed.

When comparing the designed floating point multiplier with floating point adder composing of FIR filter in point of size. The size of floating point adder has less than one fourth when comparing size of the multiplier. Therefore, if you sacrifice a little hardware, the proposed architecture is very efficient in the point of cost to effect.

ii. MEMORY CONTROLLER

The proposed DWT encoder in this paper, users can obtain a wanted compression rate as only input parameter. This requires the complex memory controller. Fig. 4, 5, 6 is shown operation process of designed encoder in this paper. Fig.4 is expressed separated memory access style of input parameter. Fig.5 represents image processing process of input parameter. The filter bank processing of the parameter is represented in Fig.6. As shown in Fig.2, the memory controller is separately designed read and write address counter and all of the operation processes are sophisticatedly controlled by signal from the middle located controller. The output data from the DWT filter bank is stored in RAM by address counter increasing according to another signal notifying effect data signal. For computing two dimension DWT, however, READ operation is complex. After finishing WRITE operation of processing present data, READ address counter increase address for loading data. Due to downsampling, the Clock cycle of output data from the DWT Filter Bank is twice as small as the system clock cycle. Due to

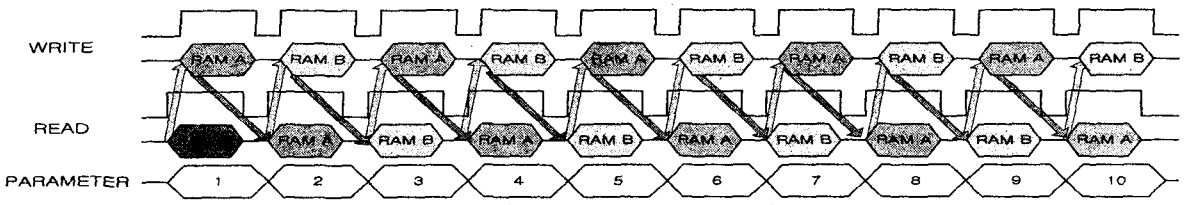

Fig. 4. Memory access style

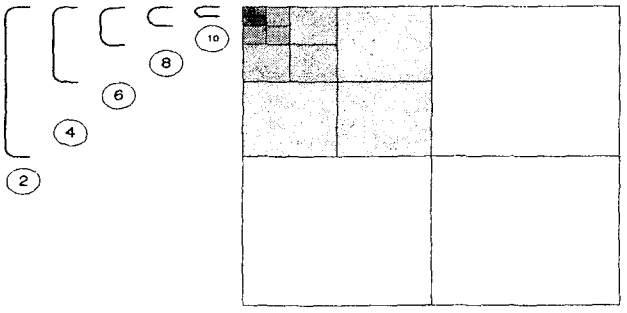

Fig. 5. Wavelet transform of image

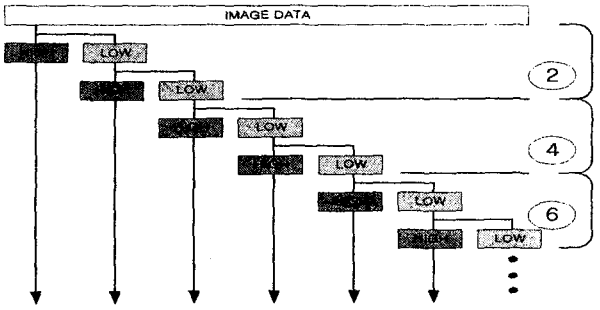

Fig. 6. Wavelet filter tree structure

READ/WRITE operation in same time, the unrighteous data may load and misoperate. The proposed encoder has respectively separated read/write address of the separated two RAM for read/write safely. The processed average signal results out through DEMUX according to input parameter.

IV. CONCLUSION

In this paper, the proposed DWT encoder can increase efficiency and users obtain a wanted compression rate with only input parameter. In the case of DWT processing using commercial DSP, it requires complex memory controller. However, the proposed encoder internally includes it to remove complex control for users. The designed encoder operates in 12MHz in the Altera FPGA chip(FLEX10K-50). If it is implemented by ASIC, it can be used on real time applications such as video processing. The proposed encoder set limits image size to 512 by 512 but it can obtains high compression rate, because it can be possible to process to max 10 stage. According to having studied results, efficient bit number for DWT filter coefficients is 12 bit but it limits 11bits because of FPGA limitation[1]. The proposed DWT encoder consists of simple architecture and can be applied easily. And it can compute lowpass and highpass DWT coefficients in the same clock cycle. As reducing half number of multiplier needed DWT computation, if implemented by ASIC for special processor, it also is very effective in the point of cost to efficiency.

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