A Simple Continuous Conduction Mode PWM Controller for Boost Power Factor Correction Converter

Tanes Tanitteerapan and Shinsaku Mori
Department of Electrical and Electronics Engineering, Faculty of Engineering,
Nippon Institute of Technology,
4-1 Gakuendai, Miyashiro-machi, Minamisaitama-gun, Saitama-ken, 345-8501, Japan
Tel. +81-480-34-4111 Ext.698, Fax.: +81-480-33-7680
e-mail : e987014@estu.nit.ac.jp, s_mori@nit.ac.jp

Abstract: This paper, a new simple controller operates in continuous conduction mode (CCM) for Boost power factor correction converter is introduced. The duty ratios are obtained by comparisons of a sensed signal from inductor current and a negative ramp carrier waveform in each switching period. By using the proposed controller, input voltage sensing, error amplifier in the current feedback loop, and analog multiplier/divider are not required, then, the control circuit implementation is very simple. To verify the proposed controller, the circuit simulation for Boost power factor correction converter was applied. For the results, the input current waveform was shaped to be closely sinusoidal, implying low THD.

1. Introduction

To operate the Boost PFC converter in continuous conduction mode (CCM), the controller as shown in Fig.1 [1] is traditionally applied. An input voltage sensing is required to obtain a sinusoidal reference, an analog multiplier to combine this reference with the output information, and an error amplifier in the current loop to extract the difference between the input current and the reference to generate the control signal for modulating the input current. Therefore, the circuit implementation of the conventional control technique is very complexity.

Recently, to reduce the complexity of the conventional control technique, control techniques in [2]-[6] are presented. Nonlinear carrier (NLC) controller in [2] is one of good example. The sinusoidal switch, diode or inductor current is sensed and compared with the carrier waveform in each one switching period for achieve the sinusoidal input current waveshape or high power factor condition ([2],[4]).

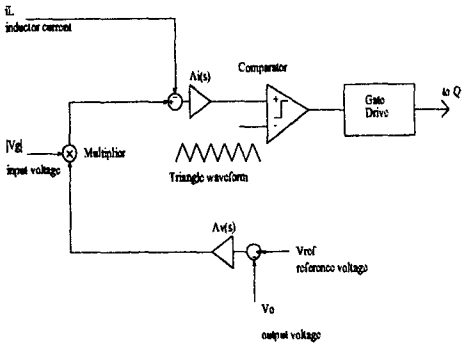

Figure 1. Conventional controller

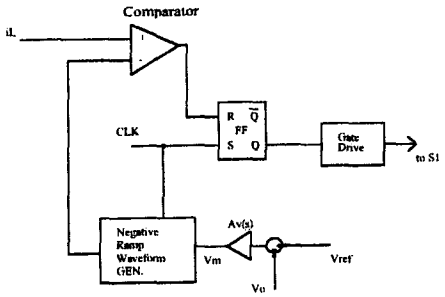

Figure 2. Proposed controller

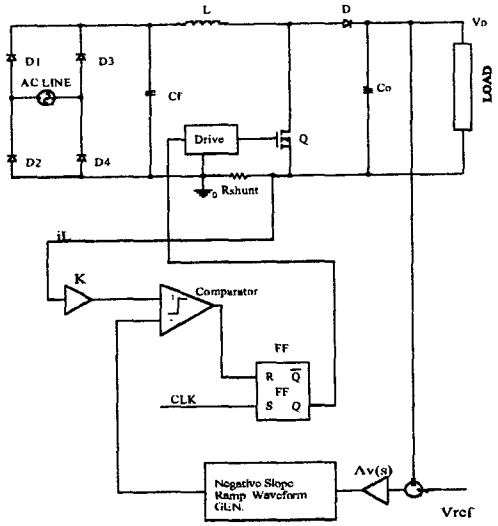

Figure3. Boost converter with proposed controller

Such NLC waveforms are derived based on the steady-stage voltage conversion thus depend on the converter topology and on which current is sensed. In other cases, a linear negative ramp carrier is employed as [6] with the aim of simplifying the carrier generator circuit.

The purpose of this paper is to present one of the simple PWM controller in CCM operation for the Boost PFC converter as shown in Fig.3. The proposed control technique is very simple, low cost. The duty ratios are determined from the comparison of the negative ramp carrier waveform and the detected signal from the inductor current. By using the proposed controller, current sensing,

input voltage sensing, error amplifier in the current feedback loop, and multiplier/divide are not required.

2. Control Circuit Operations

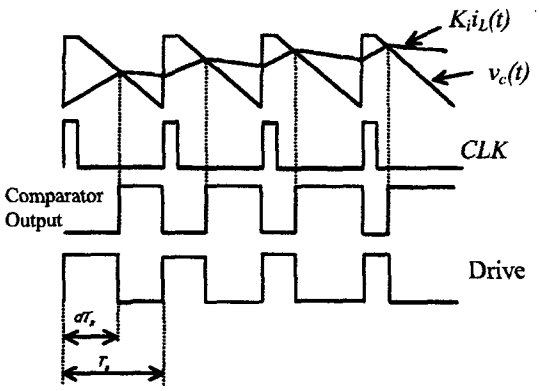

Figure 4. Control circuit operation of proposed controller

From Fig.4, at the beginning of a switching period, a short clock pulse sets the flip-flop (*FF*), which turns on the power switch *Q*. The reset of *FF* is based on the comparison of a signal $K_i i_L(t)$ from inductor current sensor and a periodic negative ramp carrier waveform $v_c(t)$ as shown in Fig. 4 (top trace). At $t = dT_s$, the carrier waveform $v_c(t)$ is equal to the signal $K_i i_L(t)$ so that the comparator output goes high and resets the *FF* turning off the power switch *Q* as shown in drive signal in Fig. 4 (lower trace). The process is repeated in each switching period.

3. Design Consideration of Proposed Controller

To implement the control circuit of the proposed controller, the steady-stage voltage conversion of Boost converter in CCM is considered that is given by

$$v_g = V_o(1-d) \qquad (1)$$

When the unity input power factor condition occurs, the emulated resistance is,

$$R_e = \frac{v_g}{i_g} \qquad (2)$$

then, when the power factor is unity, the input current is

$$i_g = \frac{V_o}{R_e}(1-d) \qquad (3)$$

Assuming input current $i_g(t)$ = inductor current $i_L(t)$ then from (16), we can directly use the relationship of inductor current to shape the input current waveform by

$$K_i i_L = \frac{V_o}{R_e}(1-d) \qquad (4)$$

where K_i is the gain of output voltage signal of inductor current sensor.

To obtain a duty *d* to satisfy (16), the voltage signal $K_i i_L$ is compared with the periodic carrier waveform $v_c(t)$ which is realized by substituting *d* with t/T_s in (16) so that,

$$v_c(t) = v_m\left[1-\frac{t}{T_s}\right] \qquad (5)$$
$$v_c(t+T_s) = v_c(t)$$

where the emulated resistance R_e is

$$R_e = \frac{V_o}{v_m} \qquad (6)$$

4. Implementation of Negative Slope Ramp Carrier Waveform Generating Circuit

To implement the negative slope ramp waveform generator circuit, (5) is applied for consideration. Firstly, the control signal v_m is integrated by using the well-known inverting integral with reset clock circuit for creating $-\frac{v_m}{T_s}t$ term that

$$v_1(t) = -\frac{1}{T_s}\int_0^{dT_s} v_m(\tau)d\tau = -\frac{v_m}{T_s}t \qquad (7)$$

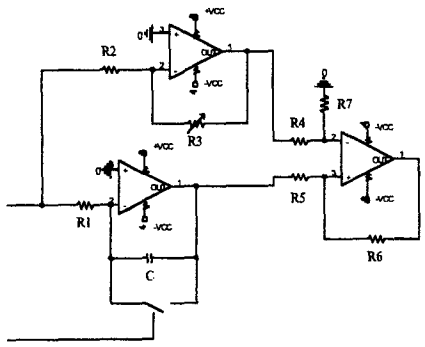

Figure 5. Implementation of negative slope ramp generator

and at the same time v_m is amplified by -1 gain then,

$$v_2(t) = -1 \times v_m = -v_m \qquad (8)$$

and both signals are compared by using the differential amplifier.

$$v_c(t) = [v_1(t) - v_2(t)] = \left[-\frac{v_m}{T_s}t + v_m\right] \qquad (9)$$
$$v_c(t) = v_m\left[1-\frac{t}{T_s}\right]$$

The circuit implementation of the negative slope ramp waveform generator in (5) is already shown in Fig.5.

5. Boundaries between CCM and DCM Operations in Proposed Controller

To determine the boundaries between CCM and DCM operations of the boost rectifier circuit with proposed controller as shown in fig.3, firstly, the duty ratio must be determined.

In the analysis, we use the following notation for normalized input voltage, v_g and the peak value of the input voltage, $V_{g,peak}$

Then,

$$m_g = \frac{v_g}{V_o} \tag{10}$$

$$M_g = \frac{V_{g,peak}}{V_o} \tag{11}$$

where m_g is conversion ratio and M_g is maximum value of the conversion ratio.

So, the duty ratio d can be determined from

$$d(t) = 1 - m_g \tag{12}$$

(12)is used to make the plots of duty ratios at several values of the conversion ratio M_g and these plots are shown in Fig.7. Here, at the large value of M_g, the maximum value of the duty ratio is low.

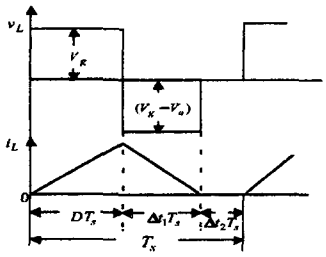

Figure 6. Inductor voltage and inductor current waveforms of the power circuit in fig.1 when operating in DCM

From the inductor current waveforms in DCM operation in fig.6, the boost rectifier will be operated in DCM when

$$\Delta t_1 < D' \tag{13}$$

and operated in CCM when

$$\Delta t_1 \geq D' \tag{14}$$

by the time interval Δt_1 is

$$\Delta t_1 = \frac{2LI_o}{V_g D T_s} \tag{15}$$

Then,

$$\begin{aligned} K < K_{crit} &\rightarrow in\ DCM\ operation \\ K > K_{crit} &\rightarrow in\ CCM\ operation \end{aligned} \tag{16}$$

where the load parameter K is defined as

$$K = \frac{2L}{RT_s} \tag{17}$$

and the boundary parameter K_{crit} is defined as

$$K_{crit} = DD'^2 \tag{18}$$

The relation in (16) and the values of duty ratio $d(t)$ from (12) are used in (18) to make the plots of K_{crit} in several conversion ratio M_g values as shown in fig.8.Here, the value of K_{crit} will be high when use the converter having high conversion ratio.

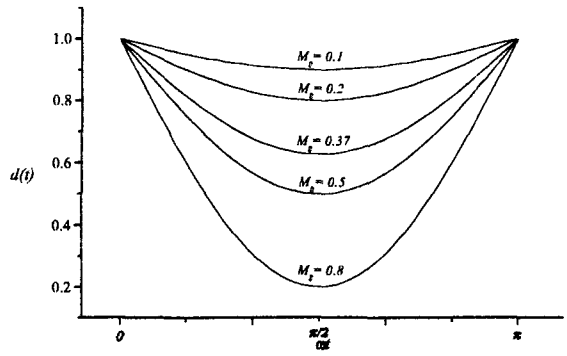

Figure.7 Theoretical plots of duty ratios $d(t)$ at several conversion ratio M_g values

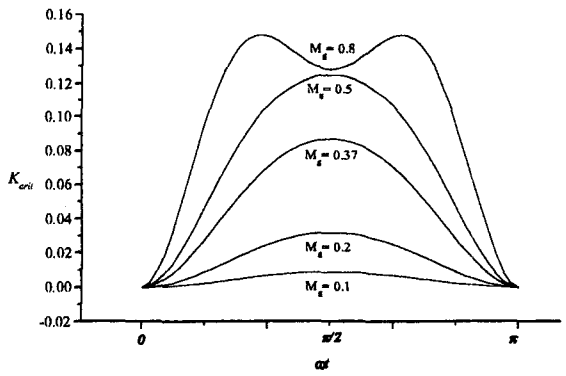

Figure.8 Theoretical plots of boundary parameters K_{crit} at several conversion ratio M_g values

6. Simulation Verifications

To verify the boost PFC converter with proposed controller, the circuit simulation on PSPIE program was applied to the circuit shown in Fig. 3 by designing to meet the following specifications:

Output power $P_o = 152\ W$
Output voltage $V_o = 380\ V_{dc}$
Input voltage $V_g = 100\ V_{rms}$
Line frequency $f = 50\ Hz$
Switching frequency $f_s = 40\ kHz$

From circuit specifications, the power circuit conversion ratio M_g is

$$M_g = \frac{\sqrt{2}V_{g,rms}}{V_o} = \frac{\sqrt{2}\times 100}{380} = 0.37$$

To ensure that the control circuit will perform the power circuit always operating in the *CCM*, the value of load parameter K must be always higher than the value of the boundary parameter K_{crit}. So, we use the boost Inductance L = 2 mH that has K = 0.168 at full load resistance = 950 Ω. Fig. 8 shows that at M_g = 0.37, the maximum value of K is about 0.08. So, the values of K are always higher than the values of K_{crit}. Then, the CCM operation can be satisfied at all full load.

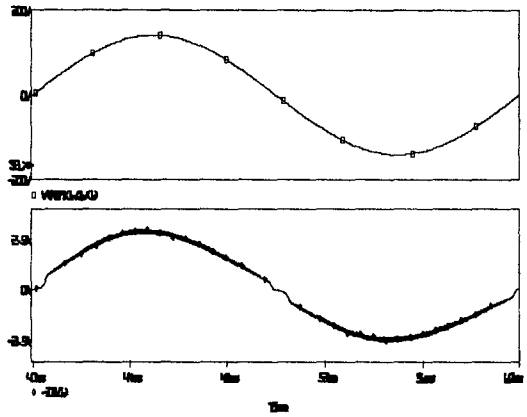

Figure 9. Simulation waveforms of (topper) input voltage, and (lower) input

By using the proposed controller, the input current is shaped to be closely sinusoidal as shown in Fig.9 (lower trace), implying low THD, high power factor and controlled in CCM operation as shown in Fig.10. In Fig.10, the controller operation waveforms are shown.

7.Conclusion

By using the proposed controllers, its operation requires only output voltage and sensed inductor current signals. So, the error amplifier in the current feedback loop, input voltage sensor, and analog multiplier, which are used in the conventional controller in Fig.1 are not required. The duty ratios are determined by comparing the sensed inductor current with the negative slope ramp signal in each switching period as shown in the simulation results in Fig.9. Therefore, its circuit implementation is very simple. By using the operation as shown in Fig.10, the input current of Boost PFC AC-to-DC converter in Fig.3 is shaped to be closely sinusoidal by following the input voltage waveform as shown in Fig.9.

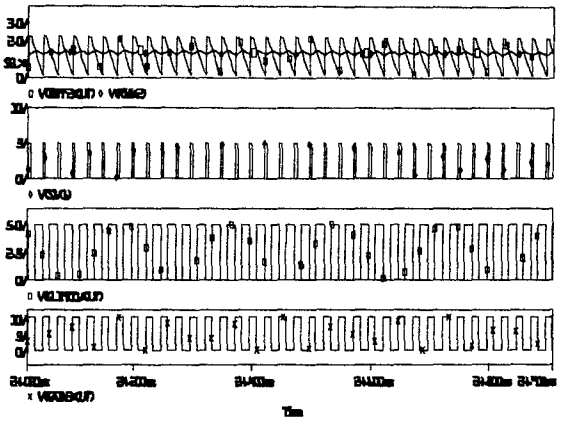

Figure 10. Simulation waveforms of the proposed controller (from the top) comparison of the negative slope ramp carrier waveform and signal from inductor current sensor, Clock signal at 40 kHz, Output signal from the comparator, and Gate driving signal respectively.

References

[1] M. Kazerani, P.D.Ziogas and G.Joos, "A novel active current waveshaping technique for solid-state input power factor conditioners," *IEEE Trans. Industry Electronics*, vol.38, no.1, February 1991.

[2] R. Zane and D. Maksimovic, "Nonlinear-Carrier Control for High Power Factor Based on Up-Down Switching Converters," *IEEE Trans. Power Electronics*, vol. 13, No. 2, March 1998, pp. 213-221.

[3] S. Buso, G.Spiazzi and D.Tagliavia,"Simplified Control Technique for High-Power Factor Flyback and Sepic Rectifiers Operating in CCM," *Industry Applications Conference*, 1999. Thirty-Fourth IAS Annual Meeting. Conference Record of the 1999 IEEE, Volume: 3, 1999 Page(s): 1633 -1638 vol.3

[4] J. Hwang, A. Chee and W. H. Ki "New Universal Control Methods for Power factor Correction and DC to DC Converter Application," *Applied Power Electronics Conference and Exposition*, 1997. APEC '97 Conference Proceedings 1997, Twelfth Annual, Volume: 1, 1997 Page(s): 59 -65 vol.1.

[5] Z.Lai and K.M. Smedley, " A family of continuous conduction mode power factor correction controller based on the general pulse width modulator," *IEEE Tran. Power Electronics*, vol.13, no.3, May 1998

[6] J. R Gegner, C. Q. Lee, " Linear Peak Current Mode Control: A Simple Active Power Factor Correction Control Technique for Continuous Conduction Mode," *Power Electronics Speasialist Conference.*, 1996, PESC'96 Conference Proceedings 1996, pp. 196-202.

[7] T. Tanitteerapan and S. Mori, " Simplified Input Current Waveshaping Technique by Using Inductor Voltage Sensing for High Power Factor Isolated Sepic, Cuk and Flyback rectifiers," *Applied Power Electronics Conference and Exposition*, 2002. APEC '02 Conference Proceedings 2002, Seventh Annual, Volume: 2, 2002 Page(s): 1208 -1214 vol.2.