Novel Gate Driving Circuit for a Ring Type SC Power Supply

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Abstract: A switched-capacitor(SC) type DC-DC converter having capability of integrated circuit fabrication have been marked for the application of mobile equipments. Especially, a ring type SC power supply is featured by the flexible and dynamic voltage conversion ratio change.

In this paper, an improvement of the gate driving techniques is proposed for high power efficiency and less area occupation on the chip. Furthermore, its power-saving operation in the stand-by state is proposed.

The three-capacitors ring type power supply is really designed and discussed. As results, the simulation results shows the high efficiency of 92.1%, and the higher output put voltage of 10.5 V compared with conventional one of 8.6 V.

1. Introduction

The popularization of low power, low voltage mobile equipments may stimulate the new generation of their power supply system. Such features as small-size, light-weight, low voltage operation, high conversion efficiency, power-saving (standby) operation and so on, are extensively requested. An SC (switched-capacitor) power supply is distinguished by the fabrication capability in an IC (integrated circuit) form and the low inductive noises, since it is mainly constructed by switches and capacitors only.

In an SC power supply, many MOSFETs are employed for the exchange of the circuit configuration. Their on-resistance characteristics affect directly the power conversion efficiency. From this reason, n-channel MOSFETs are employed as the switches because of the lower on-resistance than p-channel MOSFETs' by almost a half. Furthermore, a MOSFET gives further low on-resistance when it is driven by a high gate-to-source voltage. This latter requirement is solved by itself by using the boot-up voltage in a boot-up power supply. But in a step-down power supply, any voltage higher than the power source can not be utilized. For this solution, several effective driving methods such as high-side drivers(ex. IR2110), bootstrap circuits and so on, have been developed and used frequently in commercial power supplies, in order to obtain an excess voltage of several volts over the power source.

In this paper, a novel gate-driving circuit with less area occupation on a chip and an excess voltage generator, which is modified easily by making the best use of a ring type power supply, is proposed. Additionally, a standby power-saving operation is also proposed and discussed. At the end, the verifications are confirmed by using simulation results.

2. Conventional ring type SC power supply[1]

The circuit configuration of a conventional 3-capacitors ring type SC power supply is shown in Fig.1. The circuit symbols $\boxed{\Phi_1}$ ~ $\boxed{\Phi_{o3}}$ in the figure show MOSFET switches which are driven by the clock signals Φ_1 ~ Φ_{o3} shown in Fig.2, respectively. The following is the operation summary of the ring type power supply.

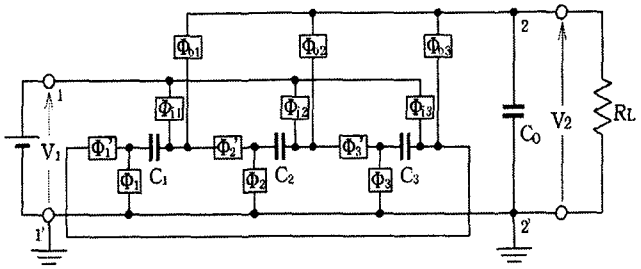

Fig. 1 Conventional 3-capacitors ring type SC power supply.

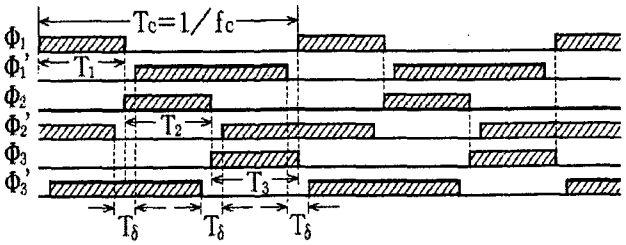

Fig. 2 Clock signals of conventional ring type SC power supply (3 times boot-up).

The switches $\boxed{\Phi_1}$ ~ $\boxed{\Phi_3}$ are called as grounded switches and driven by non-overlapped clocks with 3 phases. The switches $\boxed{\Phi'_1}$ ~ $\boxed{\Phi'_3}$ for connection of the ring are called as ring-connected switches and driven by the inverse clock signals of clocks Φ_1 ~ Φ_3. Therefore, the sequence of the spontaneous capacitor connection varies from $C_1C_2C_3$, $C_2C_3C_1$, $C_3C_1C_2$, and the repeat. The most-left capacitor of each state is grounded.

The input-side switches $\boxed{\Phi_{i1}}$ ~ $\boxed{\Phi_{i3}}$ and the output-side switches $\boxed{\Phi_{o1}}$ ~ $\boxed{\Phi_{o3}}$ are driven by clock signals which are obtained through the clock shift circuit shown in Fig.3. Namely, in case of the same phase between the input-side clocks Φ_{i1} ~ Φ_{i3} and the clocksΦ_1 ~ Φ_3, one capacitor among C_1, C_2 and C_3 is connected to the input power source V_1. In case that the clocksΦ_{i1} ~ Φ_{i3} lag behind Φ_1 ~ Φ_3 by $T_C/3$ period, two capacitors in series are connected

to V_1. In general, in the case of the circuit configuration employing n capacitors as charge-transfer capacitors, when the input-side clocks lag behind the grounded clocks $\Phi_1 \sim \Phi_3$ by $(r - 1)T_C/n$ period, total n capacitors in series are connected to the power source V_1. Then, each capacitor is charged up to V_1/r volts.

Table 1 *Voltage conversion ratio and r, s.*

j	1	2	3	4	5	6	7	8
Ratio A_{Vj}	0.33	0.5	0.67	1	1.5	2	3	0
Input-side r	3	2	3	1	2	1	1	1
Output-side s	1	1	2	1	3	2	3	Open

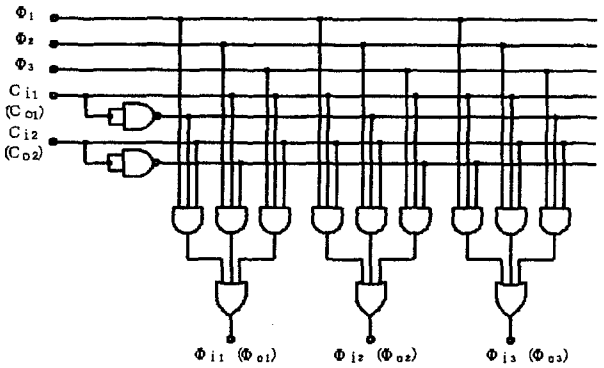

Fig. 3 *Clock shift circuit.*

Table 2 Setting of r or s.

Control bit		r or s
C_{i1} (C_{O1})	C_{i2} (C_{O2})	
0	0	Open
0	1	1
1	1	2
1	0	3

In the same matter, when the output-side clocks lag behind the grounded clocks$\Phi_1 \sim \Phi_3$ by $(s - 1)T_C/n$ period, total s capacitors in series are connected to the output terminal 2 – 2'. Therefore, the output voltage in no load state become sV_1/r. The all combinations of r and s are tabulated in Table 1, in the case that 3 charge-transfer capacitors are employed. In this table, they are arranged in the order of small conversion ratio A_{vj}. In the special case of $j = 8$, though the output-side terminal is opened, the input voltage source is connected to each capacitor and charged, which is beneficial to supply the power spontaneously to the output immediately after a power-saving state.

By using two clock shift circuits shown in Fig.3, both clock signals of the input-side clocks $\Phi_{i1} \sim \Phi_{i3}$ and the output-side clocks $\Phi o_1 \sim \Phi o_3$ can be generated, in the case of 3 charge-transfer capacitors configuration. The input signals groups C_{i1} and C_{i2}, C_{o1} and C_{o2} are control signals of 2 bit combinations of each clock and the corresponding values of r or s, are shown in Table 2. In the case that both bit are 0, all clocks become in low level, and the input and the output terminals become to be separated.

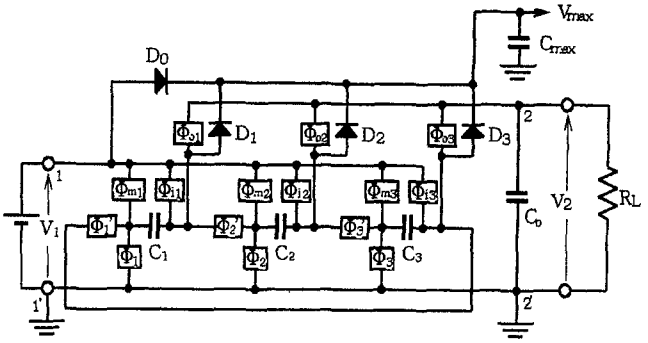

Fig. 4 Proposed SC power supply with 3-capacitor ring and simple voltage booster.

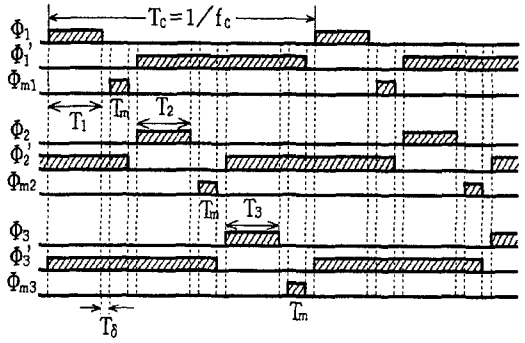

Fig. 5 Clock sequence diagram for the proposed SC power supply with 3-capacitor ring.

3. Proposed ring-type SC power supply

The proposed circuit configuration is shown in Fig. 4. It consists of the main power supply (3 times voltage supply) and the MAX circuit (4 times voltage supply). The former is a typical ring type SC power supply with a 3-capacitors ring. The latter provides the higher voltage for gate drivers, consists of 5 additional devices such as 4 diodes $D_0 \sim D_3$ and one capacitor C_{max} for a reservoir.

The output voltage of MAX circuit is estimated as followed. The capacitor C_{max} is charged to $V_1 - V_f$, where V_f is the threshold voltage of the diode ($\doteqdot$ 0.7 V), immediately after the power-on. In the steady state, each of the capacitors $C_1 \sim C_3$ is fully charged by the power source V_1. Then, the series circuit consisting of V_1 and $C_1 \sim C_3$ provides 4 times the power source V_1. Considering the V_f, it is estimated as $4V_1 - V_f$ volts.

This voltage can be obtained by using a conventional SC power supply fabricated by the side on the chip, but it may occupy more area on the chip. This additional boost circuit (MAX circuit) uses only several switches and a diode which current capacity may sufficiently small. Then this MAX circuit can be fabricated in a small area on the chip.

The driving clock sequences for the proposed circuit are shown in Fig. 5. In this figure, the clocks $\Phi_1 \sim \Phi_3$ driving the grounded-switches, the clocks driving the ring-connected switches $\Phi'_1 \sim \Phi'_3$ and the clocks driving switches of the MAX circuit $\Phi_{m1} \sim \Phi_{m3}$ are shown. The other clocks for driving the input-side switches $\Phi_{i1} \sim \Phi_{i3}$

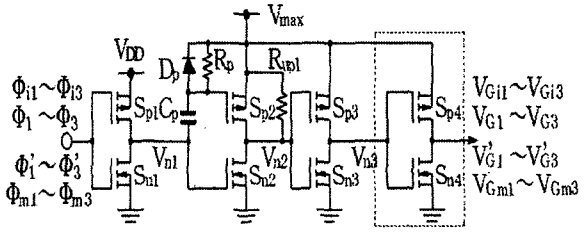

Fig. 6 Gate driver circuit for switches except output switches.

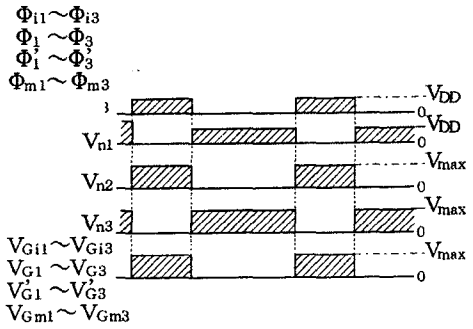

Fig. 7 Clock sequence diagram for switches except output switches.

and the output-side switches $\Phi_{o1} \sim \Phi_{o1}$ can be obtained through the clock shift circuit shown in Fig. 3. This clock sequences is very similar to the convenient SC power supply, except the clocks $\Phi_{m1} \sim \Phi_{m3}$ existing in the interval of the dead time. Then an almost same clock generator can be utilized for the additional MAX circuit. This is another advantage for adopting MAX circuit.

The 5 kinds of MOSFET switches are used in the proposed SC power supply. These switches are driven by each gate driver. Drivers for these 4 kinds of switches except output-side switches are shown in Fig.6. Then in the proposed SC power supply, 12 drivers (4 kinds ×3) of this type are used.

This circuit consists of 4 stages inverters. The first stage is fed by the power source V_1, other stages are fed by the MAX output voltage V_{max} which is almost 4 times of V_1. Therefore, two kinds of power voltages like these used, so their logic levels must be adjusted. For this purpose, a level shifter consisting of Cp, Dp and Rp is designed. This is a kind of clamp circuit.

4. Output voltage regulation

The output voltage is mainly controlled by the combination among the input-side switches and the output-side switches, that is, the s/r ratio as shown in Table

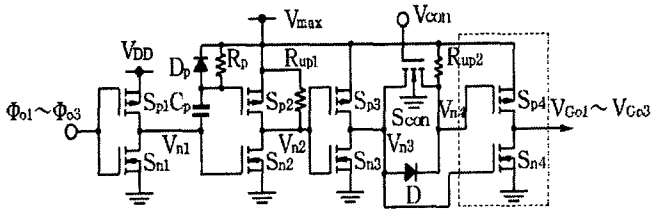

Fig. 8 Driver circuit for output switches with on-resistance control.

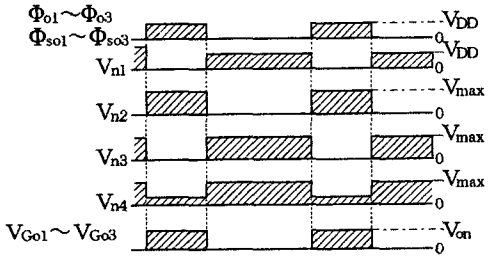

Fig. 9 Clock sequence for output switches

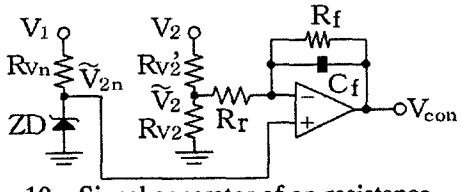

Fig. 10 Signal generator of on-resistance control.

1. More fine regulation of output voltage is made in the output-side switches. Their driver circuits and the ideal waveforms of clocks and each stage voltage are shown in Fig. 8 and Fig. 9, respectively. This driver circuit is the almost same other switched as shown in Fig. 6, except a voltage regulation circuit is inserted ahead of the last stage.

The circuit regulates the output voltage VZ by means of on-resistance control method. Namely, the on-resistance of each output-side MOSFET switches $\Phi_{o1} \sim \Phi_{o3}$ increases, when the voltage V_2 becomes high, then the output voltage V_2 is suppressed. In the Fig. 8, when the voltage V_{con} is high, the voltage V_{n4} is prevented to go down zero voltage, as shown in the fifth waveform in Fig. 9. As a result, the output voltages $V_{GO1} \sim V_{GO3}$ can not go up to the power voltage V_{max}. Furthermore, this voltage drop causes to increase the on-resistance of output-side MOSFET switches.

The on-resistance regulation method trends to increase power consumption, and to decrease the efficiency, in regular power supplies. But, in SC power supplies, the on-resistance method has the same value of efficiency, similarly to the other methods such as PWM method or the pulse frequency method, in their steady state. From the viewpoint of less noise generation and ripple voltage, this on-resistance regulation is recommended. Furthermore, the simplification of control is another advantage. Then this method is used in the proposed power supply.

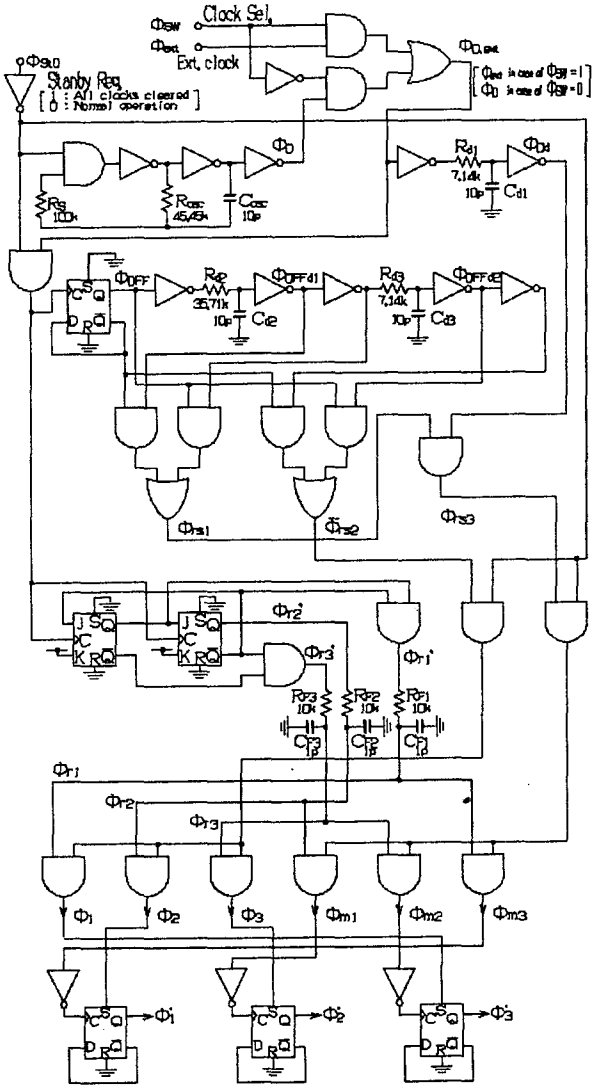

Fig. 11 Clock generator with power-saving mode.

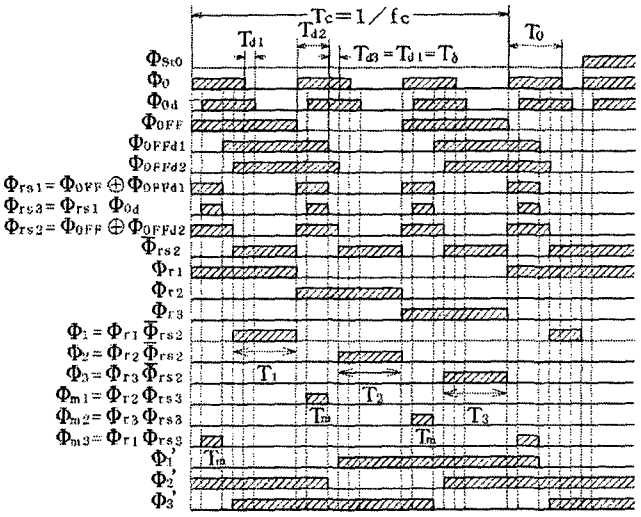

Fig. 12 *Clock sequence for generator with power-saving mode.*

Fig.10 shows the voltage comparator circuit which generates the control signal for the on-resistance regulation. The reference voltage V_{2n} and the divided output voltage V_2 are added to the error amplifier. The control voltage is obtained as its output. The relation in the stable condition is calculated from the condition that both inputs to the amplifier are equal. Then the following equation is obtained.

$$V_2 = \frac{R_{V2}}{R_{V2}+R'_{v2}} V_{2n} = V_Z \qquad (1)$$

From this relation, the output voltage V_{2n} in stable state is calculated as follows.

$$V_{2n} = \frac{R_{V2}+R'_{v2}}{R_{V2}} V_Z \qquad (2)$$

where V_Z is Zener voltage of Zener diode ZD.

5. Power-saving mode (standby mode)

It is useful that, when no load current happens, the power supply enters automatically to the power-saving mode, in order to eliminate the further power consumption. Its function is designed on the clock generator circuit shown in Fig. 11. In case that the standby signal (Φ_{STO}) becomes active, the outputs of both AND gates become low. Then all clocks become inactive (low level), and all switches turn off. As a result, the input port and the output port of the SC power supply are separated, and the great part of the clock generator enters sleep mode.

The clock sequence diagram before and after the sleep mode is shown in Fig. 12.

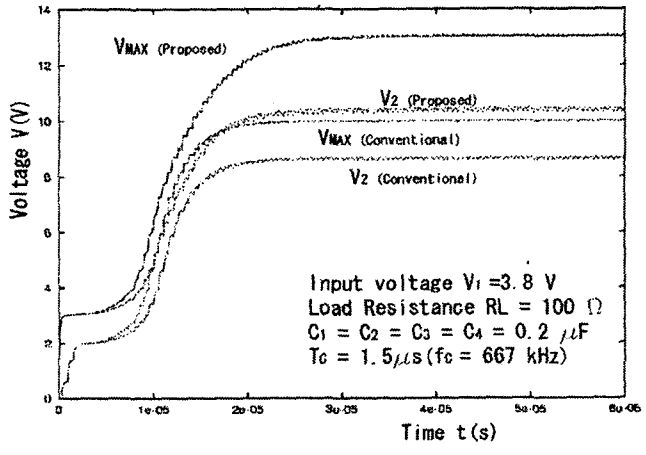

Fig. 13 Comparison between the proposed and the conventional power supplies. (3 times boot-up, and MAX outputs)

6. Circuit simulation

The characteristics of the proposed ring type SC power supply, designed as 3 times the power source voltage, which MOSFET switches are driven by using the high output voltage of MAX circuit, are compared with the conventional ring type SC power supply. Both circuits are designed to supply 3 times voltage of the power source V_1.

The simulation results are shown in Fig.13. In this simulation, the following values are used: the input voltage V_1 = 3.8 V, the load resistance R_L = 100 Ω, the charge transfer capacitors (C_1, C_2, C_3) and the reservoir capacitor (C_0) $C_1 = C_2 = C_3 = C_0 = 0.5$ μF, and the charge transfer period T_C = 1.5 μs (clock frequency f_C = 667 kHz).

The results in the conventional one show that the gate driving voltage arises to only 10 V, this insufficient driving voltage effects to the comparatively low output voltage of 8.6 V.

The power conversion ratio η is defined as follows.

$$\eta = \frac{P_2}{P_1} \times 100 = \frac{V_2 I_2}{V_1 I_1} \times 100 \quad (\%) \qquad (3)$$

In the SC power supply supplying 3 times the power source, the relation of the input and the output currents is given by $I_1 = 3I_2$, which is independent of the on-resistance of switches, the capacitance of charge transfer capacitors and clock frequency. Therefore, the efficiency is simplified as follows.

$$\eta = \frac{V_2}{3 V_1} \times 100 \quad (\%) \qquad (4)$$

In the convenient case, the efficiency is calculated as η = 75.4 % by substituting 3.8 V and 8.6 V for V_1 and V_2, respectively.

On the other hand, in the proposed power supply, the obtained gate driving voltage V_{max} = 14.1 V as a result of using MAX circuit, the output voltage V_2 = 10.5 V are obtained. The conversion efficiency η is calculated as η = 92.1 %, by substitution these values for the former equation. This calculated high efficiency shows the distinguished effect for the MAX circuit.

7. Conclusions

A novel driving method using a boosted high voltage is proposed for a ring-type SC power supply operating in a low voltage. The proposed circuit is shown to provide sufficient high voltage to gate drivers. Therefore the DC-DC converter using the proposed gate driver it gives a high conversion efficiency of 92% under the power source voltage of 3.8V. The proposed driving circuit is shown to make the best use of a ring-type SC power supply. The additional circuit can be constructed by several switches and one capacitor only.

Secondly, a power-saving mode of the gate driver circuit is proposed for the purpose to reduce the power consumption in the standby mode. This performs to make all clocks (driving signals) inactive according to the standby signal, therefore the all switches turn off and the input/output terminals are separate from the power source and the load.

Reference

[1] N. Hara, etc: Programmable ring type switched-capacitor DC-DC converters, Trans. of IEICE, Vol.J82-C-II, No.2, 56-68, 1999.