Polysilicon Thin Film Transistor for Improving Reliability using by LDD Structure

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Abstract: In this paper, Amorphous silicon on glass substrate was recrystallized to poly-crystalline silicon by solid phase crystallization (SPC) technology. The active region of thin film transistor (TFT) was fabricated by amorphous silicon. The output and transfer characteristics of thin film transistor with lightly doped drain (LDD) structure was measured and analyzed.

As a results, analyzed TFT's reliability with LDD's length by various kinds argument such as sub-threshold swing coefficient, mobility and threshold voltages were evaluated. Stress effects in TFT were able to improve to the characteristics of turn-on current and hot carrier effects by LDD's length variations..

1. Introduction

As polycrystalline silicon thin film transistor can be processed at low temperature, it is utilized in many cases when glass substrate is used as baseplate or the circuit is formed by multi-layer structure. Thin film transistor is used in many fields such as fabricating 3-dimensional integrated circuit, the element of flat board screen, the load element of high-speed SRAM, etc., and has many advantages than using amorphous silicon (A-si) thin transistor. Also, the most widely used method as a means to fabricate polycrystalline silicon thin transistor of good quality at low temperature until now is to utilize laser annealing or rapid thermal annealing (RTA) has the problem of uniformity of polycrystalline silicon on the facing area substrate and productivity, while the solid phase crystallization (SPC) method requires longer processing time than these methods, but has advantages of having excellent uniformity and remergence nature, so it is widely used. Also, as polycrystalline silicon thin film transistor has higher critical voltage than general MOS element, it has operating point of higher than 15V. As high voltage and the size of element becomes smaller, influenced much by hot carrier stress and kink effect, the reliability of element becomes to be reduced.

Also, influenced by trap existing on the boundary of grain and channel, leaking current appears much than MOS. The using method in order to reduce such degradation characteristics is inducement of lightly doped drain (LDD) structure. In this paper, by fabricating n-channel polycrystalline silicon thin film transistor of top gate structure fabricated by utilizing solid phase crystallization (SPC) of low temperature process on the glass substrate, output characteristics and transmission characteristics of element following LDD was analyzed and the changing characteristics following electrical stress was analyzed.

2. The Main Discourse

2.1 Fabricating Process of Element

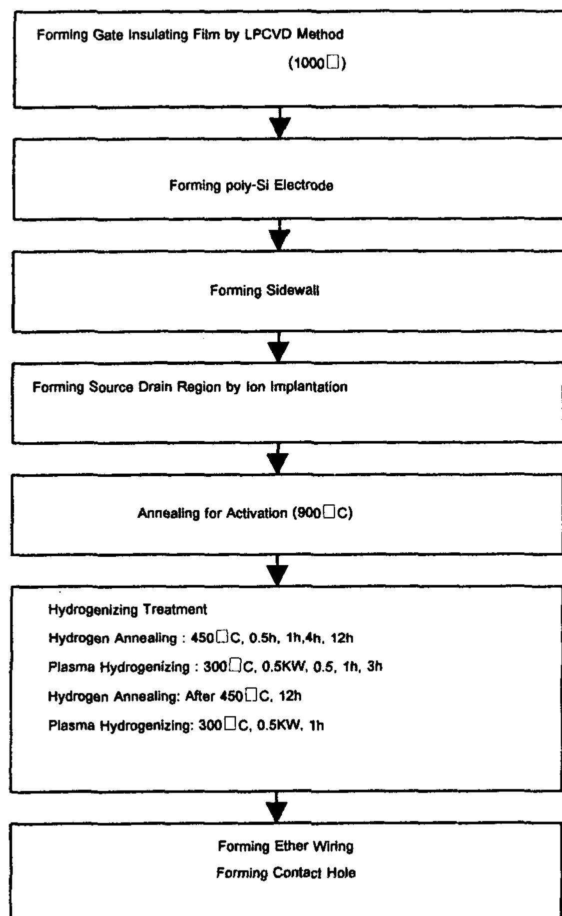

Fig. 1 Chart of Process Sequence

Fig. 1 is the process sequence in order to fabricate element for this study, and this polycrystalline silicon TFT was fabricated by the low temperature process technology (□600□C) on the glass substrate.

After forming polycrystalline silicon thin film, the gate insulation film was forced by LPCVD method, and the thickness of gate oxidized film is 1000A at that time. Then, after forming gate electrode by patterning on the gate insulation film, the estangling etching was carried out by reactive etching (RIE) by accumulating space oxidized

film, and side wall space film was forced. And, for gate electrode, phosphorus was purred in the source drain region of mask by ion pouring method, and n channel TFT was fabricated. At this time, activiting annealing was carried out at 900□C, and the ion of phosphorus pouring in condition was 80keV,3 x 1015cm-2 respectively. Also, after growing film between layers by ordinary pressure chemical weather conditional double adhering method, hydrogenous treatment was added I order reduce defect of poly-Si thin film of activated layer, and then, contact hole was formed, and metal wiring was carried out. And, for the patter of element, the length of lightly doped drain (LDD) was fabricated by 1□, 1.5 □ and 2□ respectively.

2.2 Result of Experimentation

Due to many traps on the boundary face of particle of polycrystalline silicon thin film transistor, it is greatly influenced by hot carrier stress, so leaking current is high and kink effect appears severely at high drain voltage. If LDD structure reducing side region is used for polycrystalline silicon thin film transistor, such problem points can be improved.

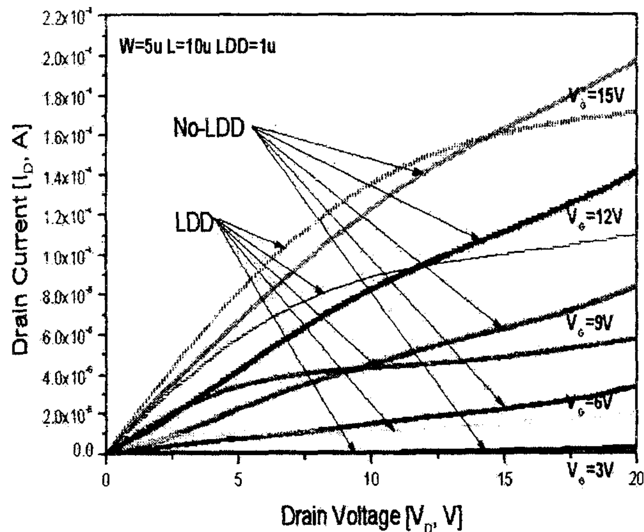

Fig. 2 ID-VD curve comparison of No-LDD and LDD

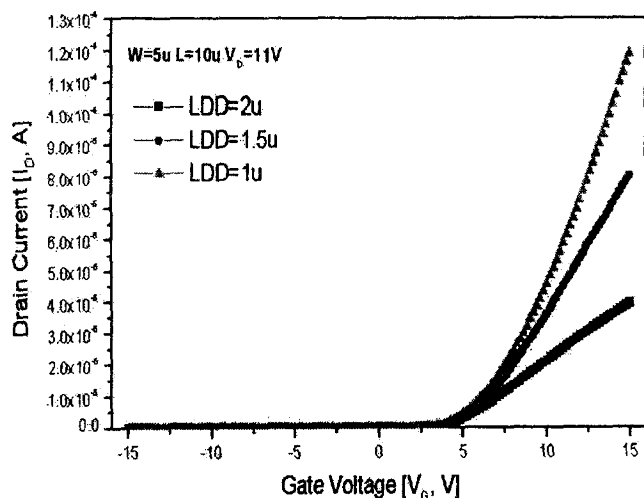

Fig. 3 ID-VG curve by LDD length

Fig. 2 shows a result showing ID-VD curve following gage of element of the length of No-LDD and LDD is 1□ when the channel width is 5□ .channel length is 10□, and as shown on the figure, it is understood that drain current of LDD shows smaller about 2.0 x 10-5 compared with NO-LDD. This is the reduction of drain current due to electrical service resistance component of LDD.

Fig. 3 is ID-VG graph following the length of LDD, and the length of LDD is 1□ and 2□. Here, the difference of driving current appeared on the length of LDD of element, which the electrical series resistance value differs according to the length of LDD, so the larger the length of LDD becomes, the larger resistance value becomes, and the driving current is reduced.

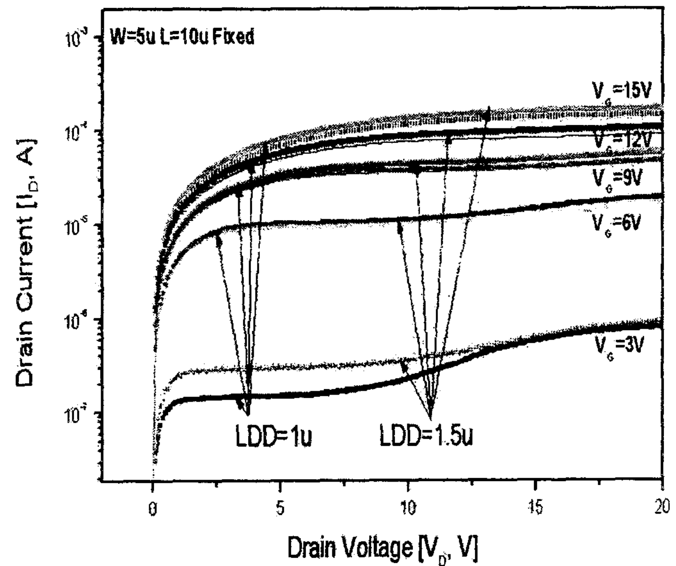

Fig. 4 ID-VD curve by LDD length variation

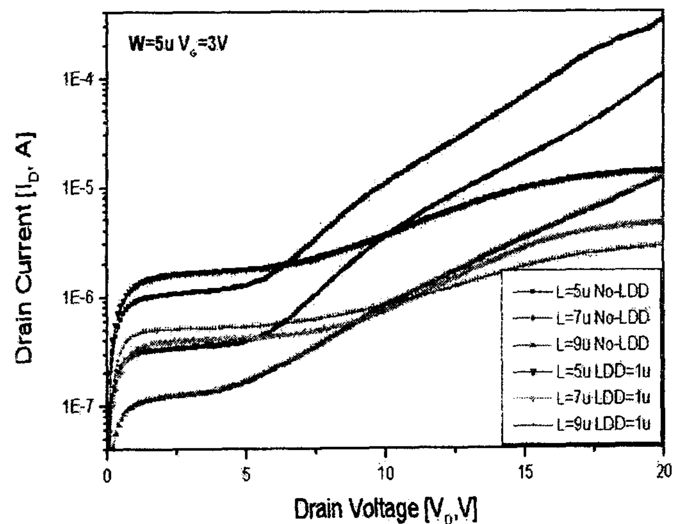

Fig. 5 Kink Currents with different channel

Fig. 4 and 5 show kink current following ID-VD curve and channel length following length of LDD, and observing Fig. 4, it can be understood that there is almost no

difference of increase of current following the length of LDD following increase of gate voltage. But, it can be observed that kink current is reduced at the longer side of LDD when gate voltage is 3V. And Fig. 5 shows kink voltage when channel width is fixed to 5□ and gate voltage to 3V and channel length was changed, and comparing when No-LDD and when LDD is 1□, it can be understood that kink voltage is remarkably reduced when it is LDD than when it is No-LDD. This is understood that it is caused by absorbing shock of strong region generated on the drain side by dispersing electronic region affecting on drain by LDD with kink current caused by increase of current by shock ionization.

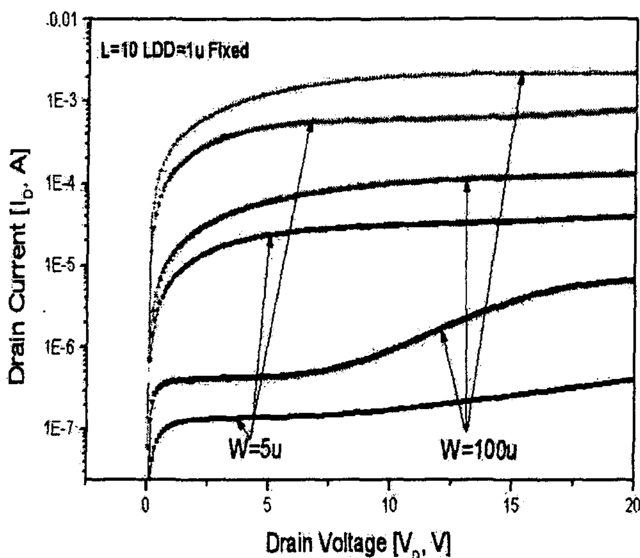

Fig. 6 ID-VD curve by channel widths

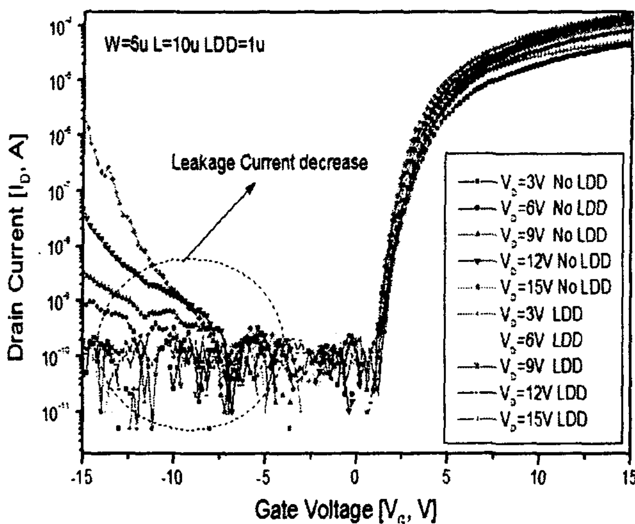

Fig. 7 ID-VD curve by decrease of leakage current

Fig. 6 shows that drain current increases much more when channel width is 100□ than 5□, which showed the tendency like the existing MOSFET. Fig. 7 is ID-VG curve following drain voltage change, and it is understood that the leakage current is reduced when LDD structure is utilized. By this, the reason can be fond from that, as mentioned before, LDD does shock absorbing action. And Fig. 8 is ID-VG curve when drain voltage is made as 15V and LDD length is made different, and electrical stress is impressed, and the stress following LDD length showed to receive less when it is 1.5□ than 1□, and if the length of LDD is too small, it cannot do stress absorbing action and showed that it received much influence by stress.

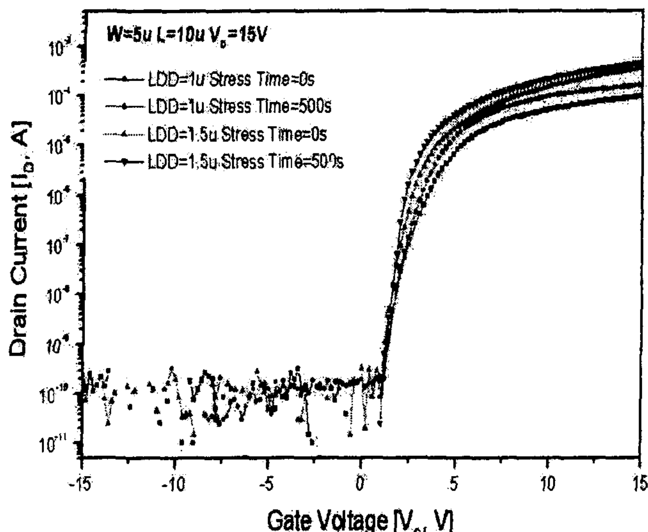

Fig. 8 ID-VD curve by electrical stress

3. Conclusion

Electrical characteristics of n channel polycrystal silicon thin film transistor with LDD structure utilizing solid phase crystallization method at low temperature below 600□C of SOI structure on grass substrate was analyzed. Observing change of output characteristics following channel width and channel length, the division of fan shape region and saturation region of large element of channel width and length appeared more clearly than small element of channel width and length, and by the length of LDD, the longer the length of LDD becomes, the electrical series resistance increased between drain and bulk and driving current was reduced, and if the length of LDD is short, stress by hot carrier due to increase of side region is to be received, so the length of LDD shall be adjusted in accordance with various conditions. It is understood that in the influence of leakage current, kink current and stress, polycrystalline silicon thin film transistor utilizing LDD structure is more improved reliability than the existing polycrystalline silicon thin film transistor.

4. Biography

□1□ Do-Hyun Baek, Yong-Jae Lee, "Stress-Bias Effect on Poly-Si TFT's of Glass Substrate", ITC-CSCC2000, Vol. 2 pp. 933-936, 2000

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